

SAPPORO 150A+G

LA-2101 REV0.1 Schematic

Portability Prescott/Northwood

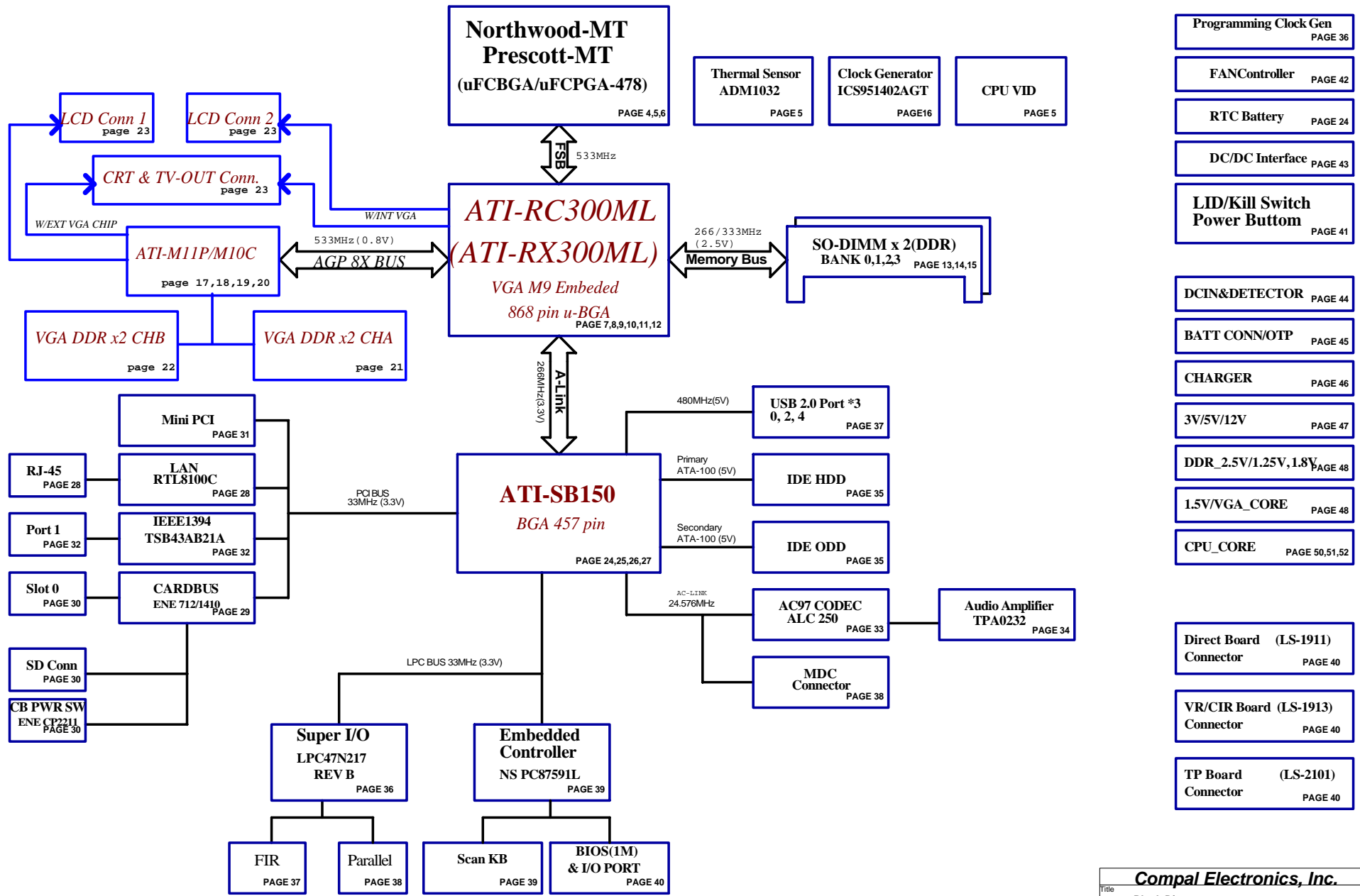
RC300ML(RX300ML)+IXP150+ATI M11P/M10C(128MB VRAM)

2003-11-10

Compal Electronics, Inc.

Title		
Cover Page		
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DAL01 LA-2101 BLOCK DIAGRAM



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X/8X	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VGA	AD16		PIRQA
CardBus	AD20	2	PIRQA
LAN	AD19	3	PIRQD
Mini-PCI	AD18	1/4	PIRQC/PIRQD
1394	AD16	0	PIRQA
SD	AD20	2	PIRQB

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b	ICS960011	1101 110X b
(24C04)	1011 000Xb		

IXP150 SM Bus address

Device	Address
Clock Generator (ICS951402AGT)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 001Xb

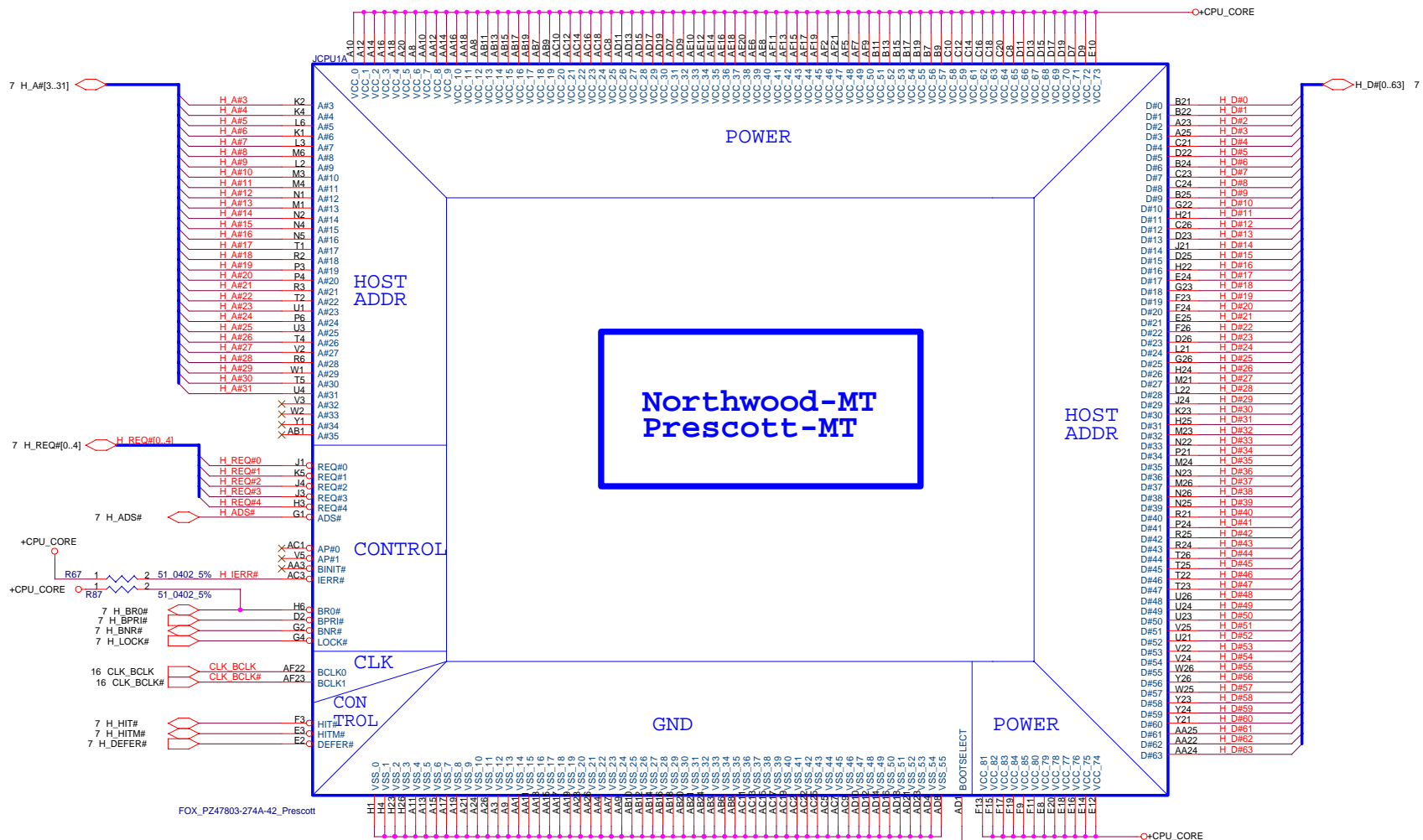
STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

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Notes		
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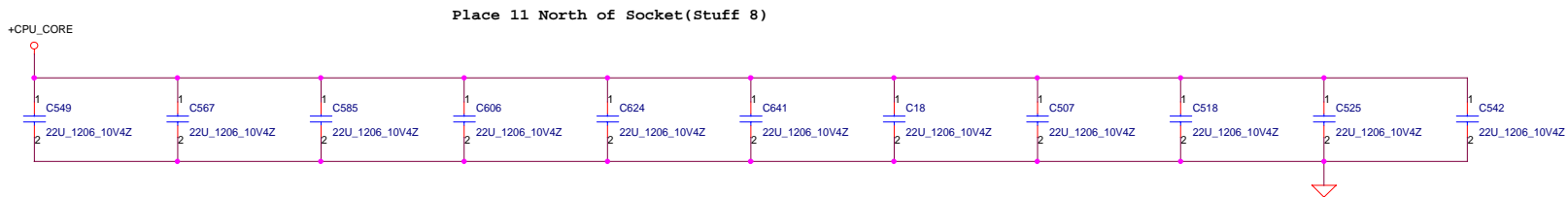


Reference Intel document
 Desktop P4 Spec.: 10988 P4 0.13u 512KB L2 EMTS Rev.2.0
 Desktop Prescott Spec.: 11910 Prescott EMTS Rev.0.5

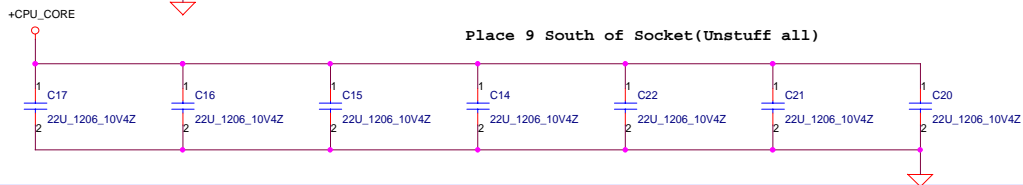
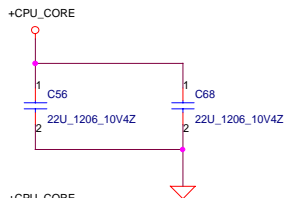
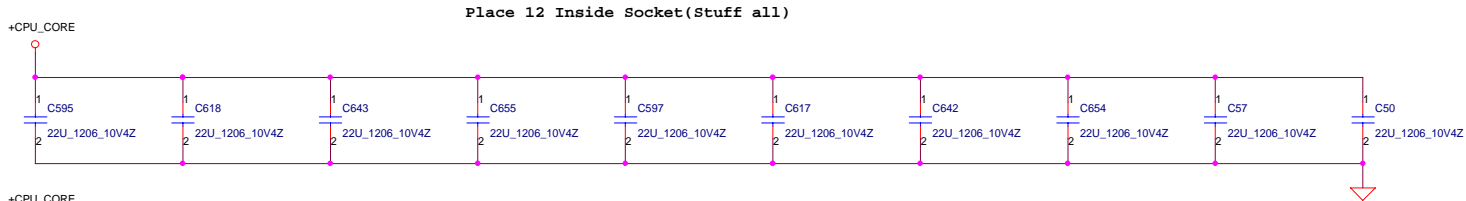
Pin number	Northwood Pin name	Comment	Prescott Pin name	Comment	Northwood	Prescott
B6	FERR#	Pull-up 62ohm to +VCC_CORE	FERR#/PBE#	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AA20	ITPCLKOUT0	Pull-up 56ohm to +VCC_CORE	TESTHI6	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AB22	ITPCLKOUT1	Pull-up 56ohm to +VCC_CORE	TESTHI7	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AD2	NC	float	VIDPWRGD	Pull-up 8.2Kohm to +VCCVID	Depop	Pop
AD3	NC	float	VID5	Pull-up 1Kohm to +3VRUN & connect to PWRIC	Depop	Pop
AF3	NC	float	VCCVIDLB	Connect to +VCCVID	Depop	Pop
AD20	VCCA	Connect to CPU Filter	VCCIOPLL	Connect to CPU Filter		
AF23	VCCIOPLL	Connect to CPU Filter	VCCA	Connect to CPU Filter		
AD1	VSS	Connect to GND	BOOTSELECT	CPU determine	Pop	Depop
AE26	VSS	Connect to GND	OPTIMIZED/COMPAT#	float	Pop	Depop

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Title Prescott Processor in uFCPGA478 (1/2)		
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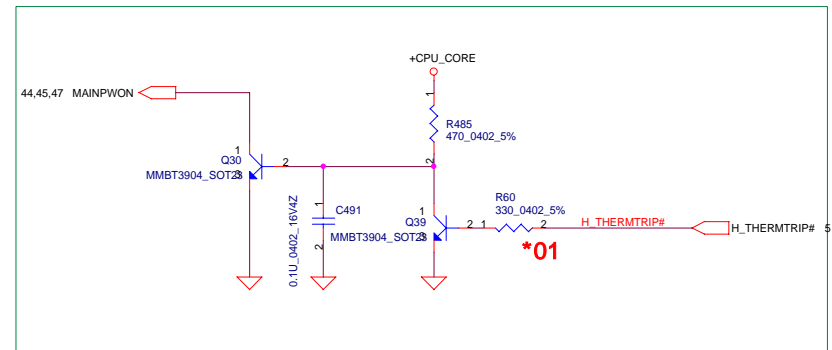
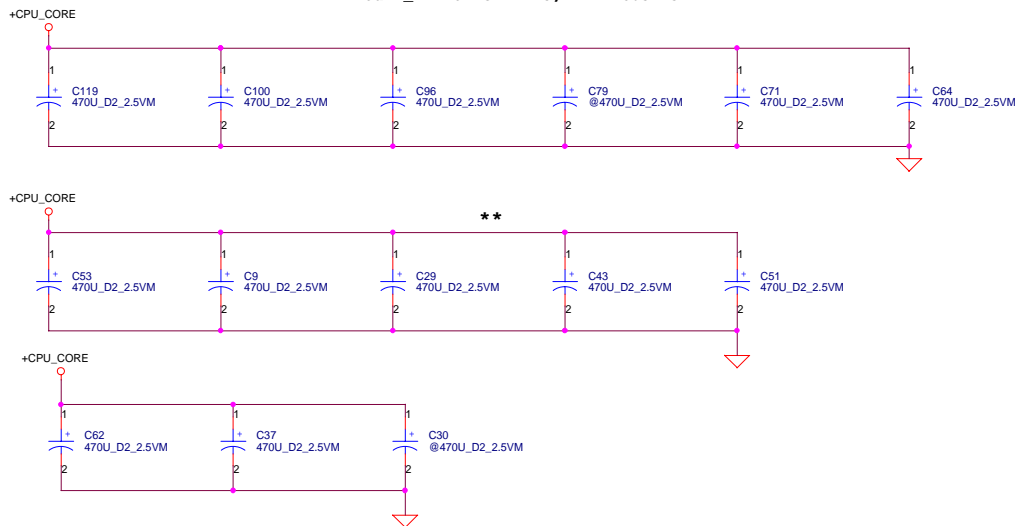
22uF depop reference
Springdale Customer Schematic R1.2 page82



Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page239

Decoupling Reference Requirement:
560uF Polymer, ESR:5m ohm(each) * 10
22uF X5R * 32

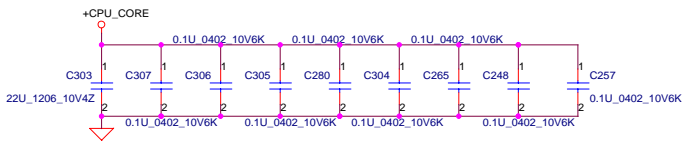
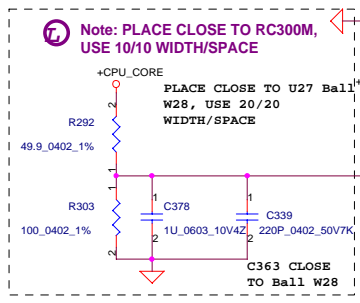
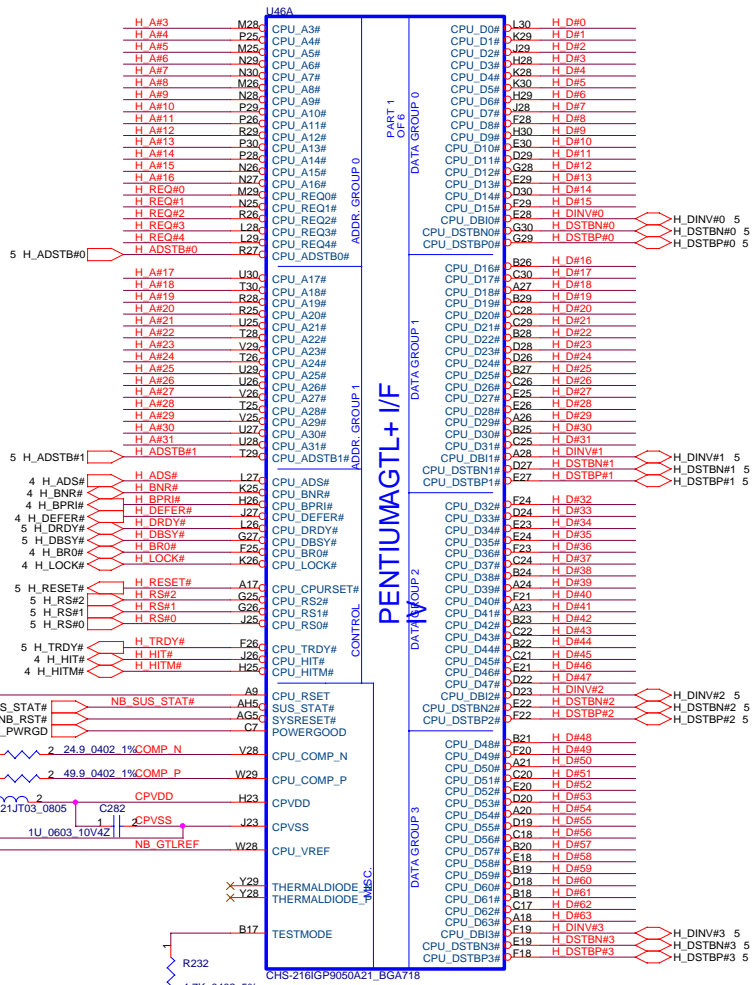
470uF _ERS10m ohm* 15, ESR=0.5m ohm



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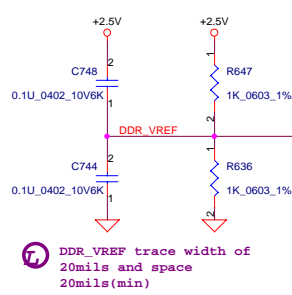
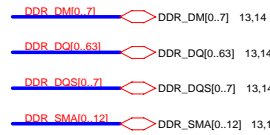
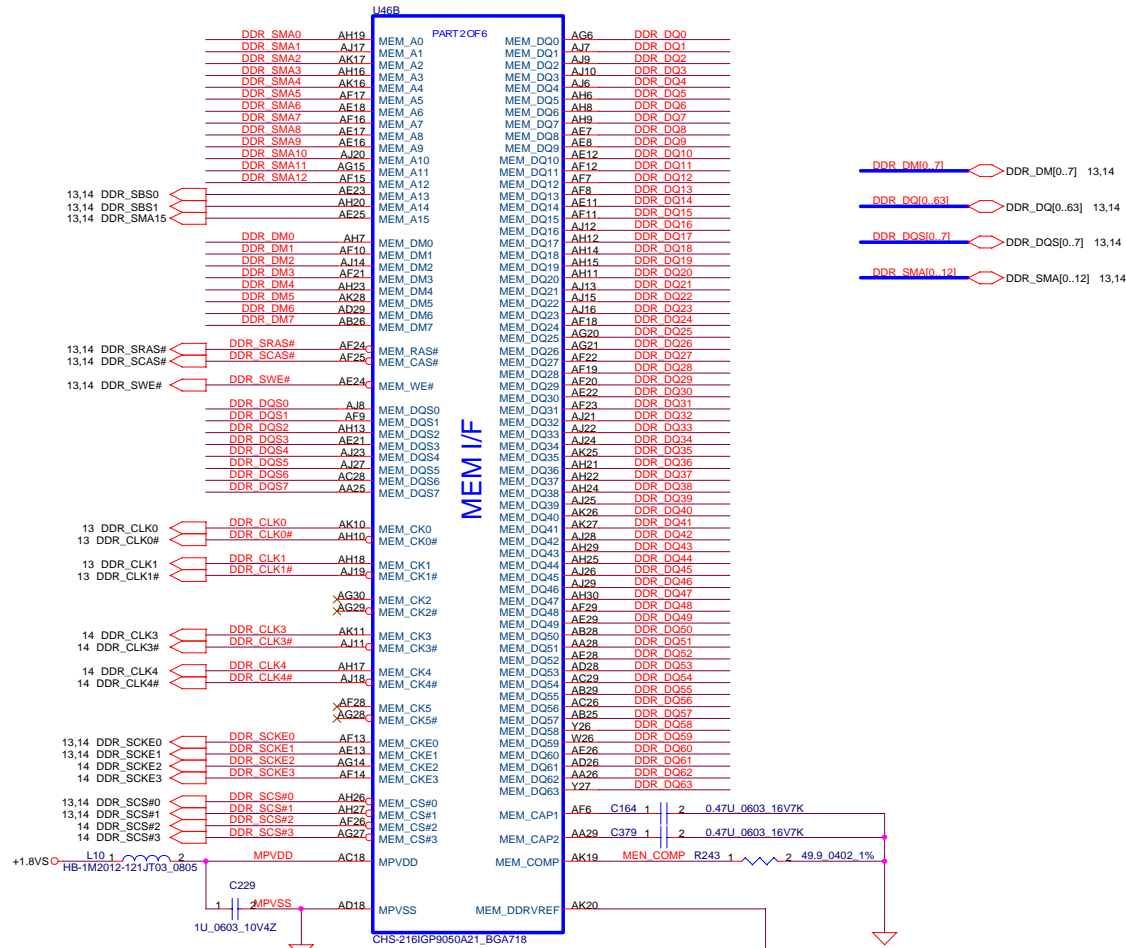
Title CPU Decoupling		
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H_A#(3..31) → H_A#(3..31) 4
 H_REQ#(0..4) → H_REQ#(0..4) 4
 H_D#(0..63) → H_D#(0..63) 4



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Title AT1RC300M-AGTL+		
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12,24 A_AD[0..31] \rightarrow A_AD[0..31]
 24 A_CBE[0..3] \rightarrow A_CBE[0..3]

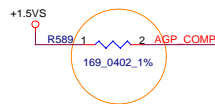
U46C
 A_AD0 AK5 ALINK_AD0
 A_AD1 AJ5 ALINK_AD1
 A_AD2 AJ4 ALINK_AD2
 A_AD3 AH4 ALINK_AD3
 A_AD4 AJ3 ALINK_AD4
 A_AD5 AJ2 ALINK_AD5
 A_AD6 AH2 ALINK_AD6
 A_AD7 AH1 ALINK_AD7
 A_AD8 AG2 ALINK_AD8
 A_AD9 AC1 ALINK_AD9
 A_AD10 AC3 ALINK_AD10
 A_AD11 AE3 ALINK_AD11
 A_AD12 AF1 ALINK_AD12
 A_AD13 AF2 ALINK_AD13
 A_AD14 AF4 ALINK_AD14
 A_AD15 AE3 ALINK_AD15
 A_AD16 AE4 ALINK_AD16
 A_AD17 AE5 ALINK_AD17
 A_AD18 AE6 ALINK_AD18
 A_AD19 AC2 ALINK_AD19
 A_AD20 AC4 ALINK_AD20
 A_AD21 AB3 ALINK_AD21
 A_AD22 AB2 ALINK_AD22
 A_AD23 AB5 ALINK_AD23
 A_AD24 AB6 ALINK_AD24
 A_AD25 AA2 ALINK_AD25
 A_AD26 AA4 ALINK_AD26
 A_AD27 AA5 ALINK_AD27
 A_AD28 AA6 ALINK_AD28
 A_AD29 Y3 ALINK_AD29
 A_AD30 Y5 ALINK_AD30
 A_AD31 Y6 ALINK_AD31

A_CBE#0 AG4 ALINK_CBE#0
 A_CBE#1 AE2 ALINK_CBE#1
 A_CBE#2 AC3 ALINK_CBE#2
 A_CBE#3 AA3 ALINK_CBE#3

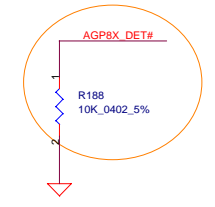
12,24 A_PAR \rightarrow A_PAR AD5 PCI_PAR/ALINK_NC
 24 A_STROBE# \rightarrow A_STROBE# AC6 PCI_FRAME#/ALINK_STROBE#
 24 A_ACAT# \rightarrow A_ACAT# AC5 PCI_IRDY#/ALINK_ACAT#
 24 A_END# \rightarrow A_END# AD2 PCI_TRDY#/ALINK_END#
 17,24,29,32 PCI_PIRQA# \rightarrow R174 2 @ 0.0402 5% W4 INTA#
 24 A_DEVSEL# \rightarrow A_DEVSEL# AD3 ALINK_DEVSEL#
 24 A_OFF# \rightarrow A_OFF# AD6 PCI_STOP#/ALINK_OFF#

24 A_SBREQ# \rightarrow A_SBREQ# W5 ALINK_SBREQ#
 24 A_SBGNT# \rightarrow A_SBGNT# W6 ALINK_SBGNT#
 +3VS \rightarrow R196 2 @ 0.0402 5% V5 PCI_REQ#/ALINK_NC
 8.2K @0.0402 5% X V6 PCI_GNT#/ALINK_NC

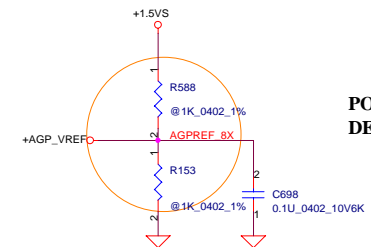
17 AGP_GNT# \rightarrow AGP_GNT# K5 AGP2_GNT#/AGP3_GNT
 17 AGP_REQ# \rightarrow AGP_REQ# K6 AGP2_REQ#/AGP3_REQ
 AGP8X_DET# M5 AGP8X_DET#
 AGPREF_8X J6 AGP_VREF/TMDS_VREF



POP For 150G
DEPOP For 150A



POP For 150G
DEPOP For 150A



POP For 150A
DEPOP For 150G

PCI Bus 0 / A-Link I/F
 PCI BUS 1 / AGP Bus (GPIO , TMDS , ZVPort)

AGP_AD0/TMD2_HS Y2 AGP_AD0
 AGP_AD1/TMD2_VS Y3 AGP_AD1
 AGP_AD2/TMD2_D1 W2 AGP_AD2
 AGP_AD3/TMD2_D0 V3 AGP_AD3
 AGP_AD4/TMD2_D3 V2 AGP_AD4
 AGP_AD5/TMD2_D2 Y1 AGP_AD5
 AGP_AD6/TMD2_D5 U1 AGP_AD6
 AGP_AD7/TMD2_D4 T2 AGP_AD7
 AGP_AD8/TMD2_D6 R2 AGP_AD8
 AGP_AD9/TMD2_D9 P3 AGP_AD9
 AGP_AD10/TMD2_D8 L2 AGP_AD10
 AGP_AD11/TMD2_D11 P2 AGP_AD11
 AGP_AD12/TMD2_D10 N3 AGP_AD12
 AGP_AD13/TMD2_D11 M3 AGP_AD13
 AGP_AD14/TMD2_D10 M2 AGP_AD14
 AGP_AD15/TMD2_D10 L1 AGP_AD15
 AGP_AD16/TMD1_VS Y3 AGP_AD16
 AGP_AD17/TMD1_HS Y3 AGP_AD17
 AGP_AD18/TMD1_HS Y3 AGP_AD18
 AGP_AD19/TMD1_DE J2 AGP_AD19
 AGP_AD20/TMD1_D1 J3 AGP_AD20
 AGP_AD21/TMD1_D2 J1 AGP_AD21
 AGP_AD22/TMD1_D3 J1 AGP_AD22
 AGP_AD23/TMD1_D4 H3 AGP_AD23
 AGP_AD24/TMD1_D7 F3 AGP_AD24
 AGP_AD25/TMD1_D6 F2 AGP_AD25
 AGP_AD26/TMD1_D9 F1 AGP_AD26
 AGP_AD27/TMD1_D8 E2 AGP_AD27
 AGP_AD28/TMD1_D11 E1 AGP_AD28
 AGP_AD29/TMD1_D10 D2 AGP_AD29
 AGP_AD30/TMDS_HF D1 AGP_AD30
 AGP_AD31/TMDS_HF D1 AGP_AD31

AGP2_SBSTB/AGP3_SBSTB/NC/LVDS_BLON E5 AGP_SB_STBF AGP_SB_STBF 17
 AGP2_SBSTB/AGP3_SBSTB/NC/ENA_BU E6 AGP_SB_STBS AGP_SB_STBS 17
 AGP2_ADSTB0/AGP3_ADSTB0/TMD2_CLK T3 AGP_AD_STBF0 AGP_AD_STBF0 17
 AGP2_ADSTB0/AGP3_ADSTB0/TMD2_CLK U2 AGP_AD_STBS0 AGP_AD_STBS0 17
 AGP2_ADSTB1/AGP3_ADSTB1/TMD1_CLK H2 AGP_AD_STBF1 AGP_AD_STBF1 17
 AGP2_ADSTB1/AGP3_ADSTB1/TMD1_CLK H2 AGP_AD_STBS1 AGP_AD_STBS1 17

AGP2_CBE#0/AGP3_CBE#0/TMD2_D7 R3 AGP_CBE#0
 AGP2_CBE#1/AGP3_CBE#1/TMD2_DE M1 AGP_CBE#1
 AGP2_CBE#2/AGP3_CBE#2 L3 AGP_CBE#2
 AGP2_CBE#3/AGP3_CBE#3/TMD1_D5 H1 AGP_CBE#3

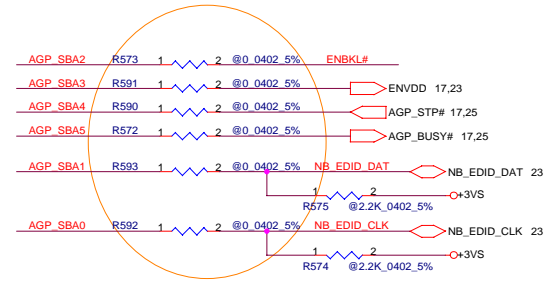
AGP2_IRDY#/AGP3_IRDY#/GPIO8/I2C_CLK P5 AGP_IRDY# AGP_IRDY# 17
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 AGP2_STOP#/AGP3_STOP#/GPIO10/DDC_DATA T6 AGP_STOP# AGP_STOP# 17
 AGP2_STOP#/AGP3_STOP#/GPIO10/DDC_DATA T6 AGP_PAR AGP_PAR 17

AGP2_FRAME#/AGP3_FRAME#/TMDS_DVI_DATA P6 AGP_FRAME# AGP_FRAME# 17
 AGP2_DEVSEL#/AGP3_DEVSEL#/GPIO9/I2C_DATA R5 AGP_DEVSEL# AGP_DEVSEL# 17
 AGP2_PIPE#/AGP3_DBI_HI D3 AGP_DBI_HI AGP_DBI_HI 17
 AGP2_NC/AGP2_DBI_LO D3 AGP_DBI_LO AGP_DBI_LO 17
 AGP2_RBF#/AGP3_RBF# N6 AGP_RBF# AGP_RBF# 17
 AGP2_WBF#/AGP3_WBF# N5 AGP_WBF# AGP_WBF# 17

AGP2_SBA0/AGP3_SBA#0/GPIO0/VDDC_CNTL C3 AGP_SBA0
 AGP2_SBA1/AGP3_SBA#1/GPIO1/VDDC_CNTL C2 AGP_SBA1
 AGP2_SBA2/AGP3_SBA#2/GPIO2/LVDS_BLON D4 AGP_SBA2
 AGP2_SBA3/AGP3_SBA#3/GPIO3/LVDS_DIGON E4 AGP_SBA3
 AGP2_SBA4/AGP3_SBA#4/GPIO4/STP_AGP F6 AGP_SBA4
 AGP2_SBA5/AGP3_SBA#5/GPIO5/AGP_BUSY F5 AGP_SBA5
 AGP2_SBA6/AGP3_SBA#6/GPIO6/LVDS_SSOUT G6 AGP_SBA6
 AGP2_SBA7/AGP3_SBA#7/GPIO7/LVDS_SIN G5 AGP_SBA7

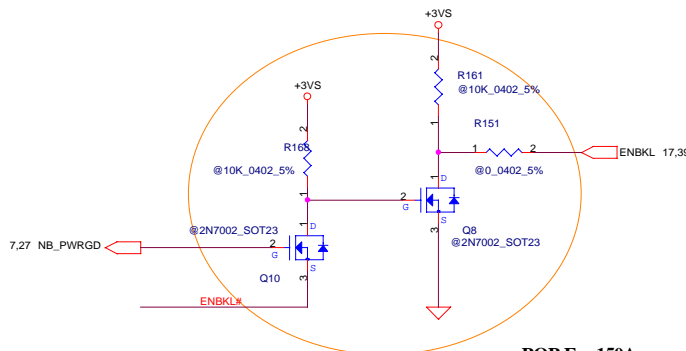
AGP_ST0 L6 AGP_ST0
 AGP_ST1 M6 AGP_ST1
 AGP_ST2 L5 AGP_ST2

AGPAND LVDS MUXED SIGNALS



POP For 150A
DEPOP For 150G

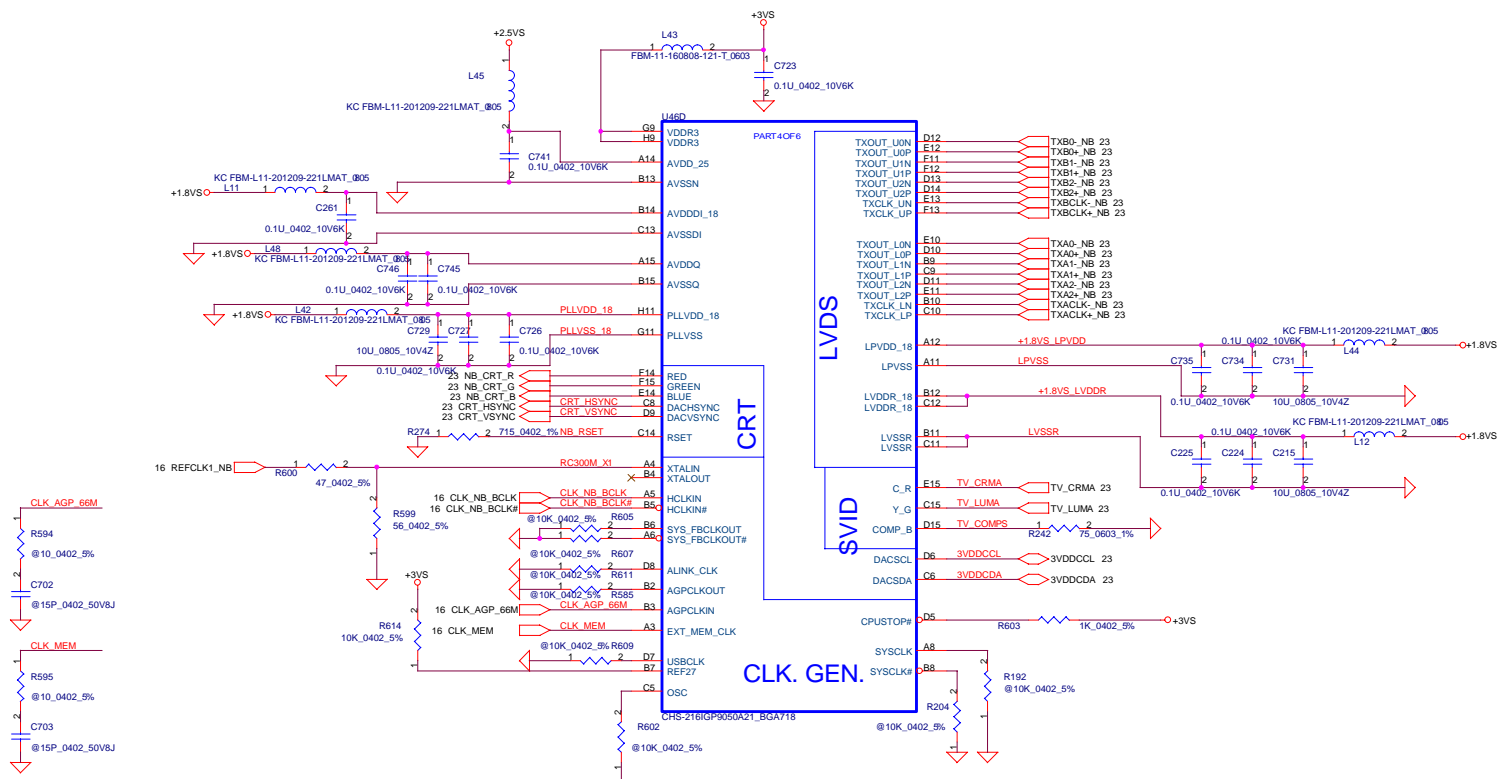
AGP_AD[0..31] \rightarrow AGP_AD[0..31] 17
 AGP_SBA[0..7] \rightarrow AGP_SBA[0..7] 17
 AGP_CBE[0..3] \rightarrow AGP_CBE[0..3] 17
 AGP_ST[0..2] \rightarrow AGP_ST[0..2] 17



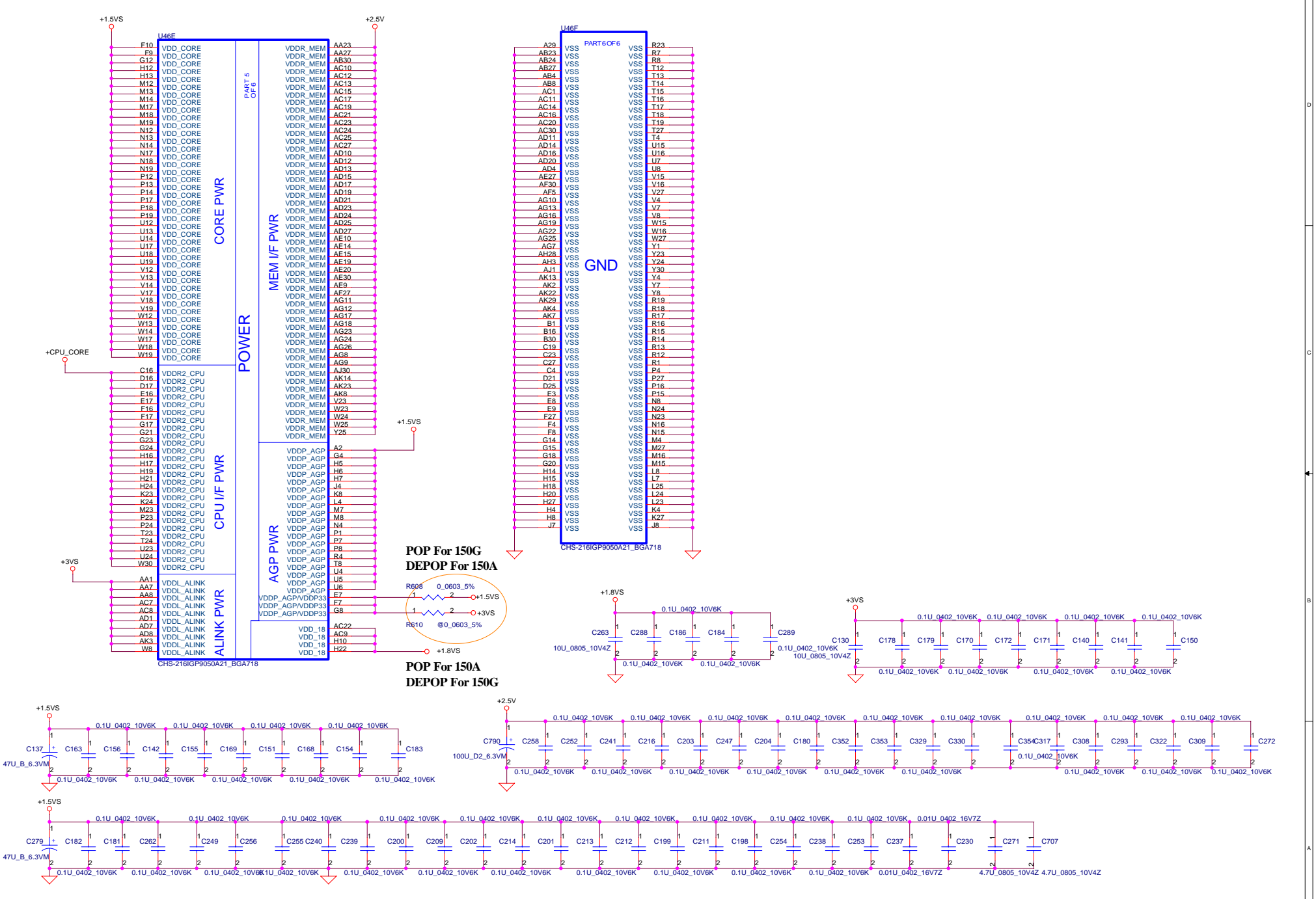
POP For 150A
DEPOP For 150G

Compal Electronics, Inc.			
ATI RC300M-AGP, ALINK BUS			
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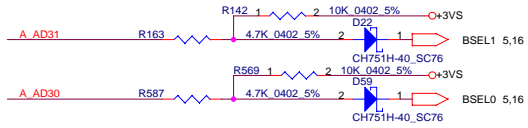
Compal Electronics, Inc.		
Title		
AT1RC300M-AGP, ALINK BUS		
Size	Document Number	Rev
	LA-2101	0.1
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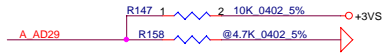
Compal Electronics, Inc.		
Title ATI RC300M-POWER		
Size	Document Number LA-2101	Rev 0.1
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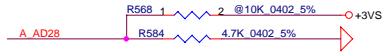
9.24 A_AD[0..31] A_AD[0..31]



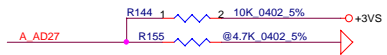
A_AD[31..30] : FSB CLK SPEED
DEFAULT: 01
 00: 100 MHZ
 01: 133 MHZ
 10: 200MHZ
 11:166 MHZ



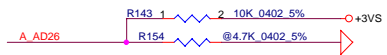
A_AD29: STRAP CONFIGURATION
DEFAULT:1
 0:REDUCEDE SET
 1: FULL SET



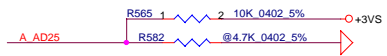
A_AD28: SPREAD SPECTRUM ENABLE
DEFAULT:0
 0: DISABLE
 1: ENABLE



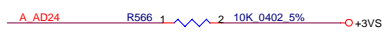
A_AD27: FrcShortReset#
DEFAULT: 1
 0: TEST MODE
 1: NORMAL MODE



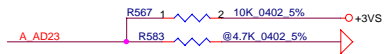
A_AD26 : ENABLE IOQ
DEFAULT: 1
 0: IOQ=1
 1: IOQ=12



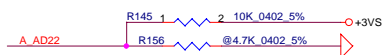
A_AD25/A_AD17 : CPU VOLTAGE[1..0]
DEFAULT: 10
 AD25=1 DESTOP CPU
 AD25=0 MOBILE CPU
 00: 1.05V
 01: 1.35V
 11: 1.75V
 10: 1.45V
 AD17--DON'T CARE



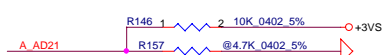
A_AD24 : MOBILE CPU SELECT
DEFAULT: 1
 0: BANIAS CPU
 1: OTHER CPU



A_AD23 : CLOCK BYPASS DISABLE
DEFAULT: 1
 0: TESTMODE
 1: NORMAL



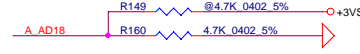
A_AD22 : OSC PAD OUTPUT PCICKL
DEFAULT : 1
 0: PCICKL OUT
 1: OSC CLK OUT



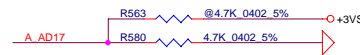
A_AD21 : AUTO_CAL ENABLE
DEFAULT : 1
 0: DISABLE
 1: ENABLE



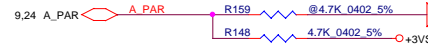
A_AD20 : INTERNAL CLK GEN ENABLE
DEFAULT : 0
 0: DISABLE
 1: ENABLE



A_AD18 : ENABLE PHASE CALIBRATION
DEFAULT: 0
 0: DISABLE
 1: ENABLE



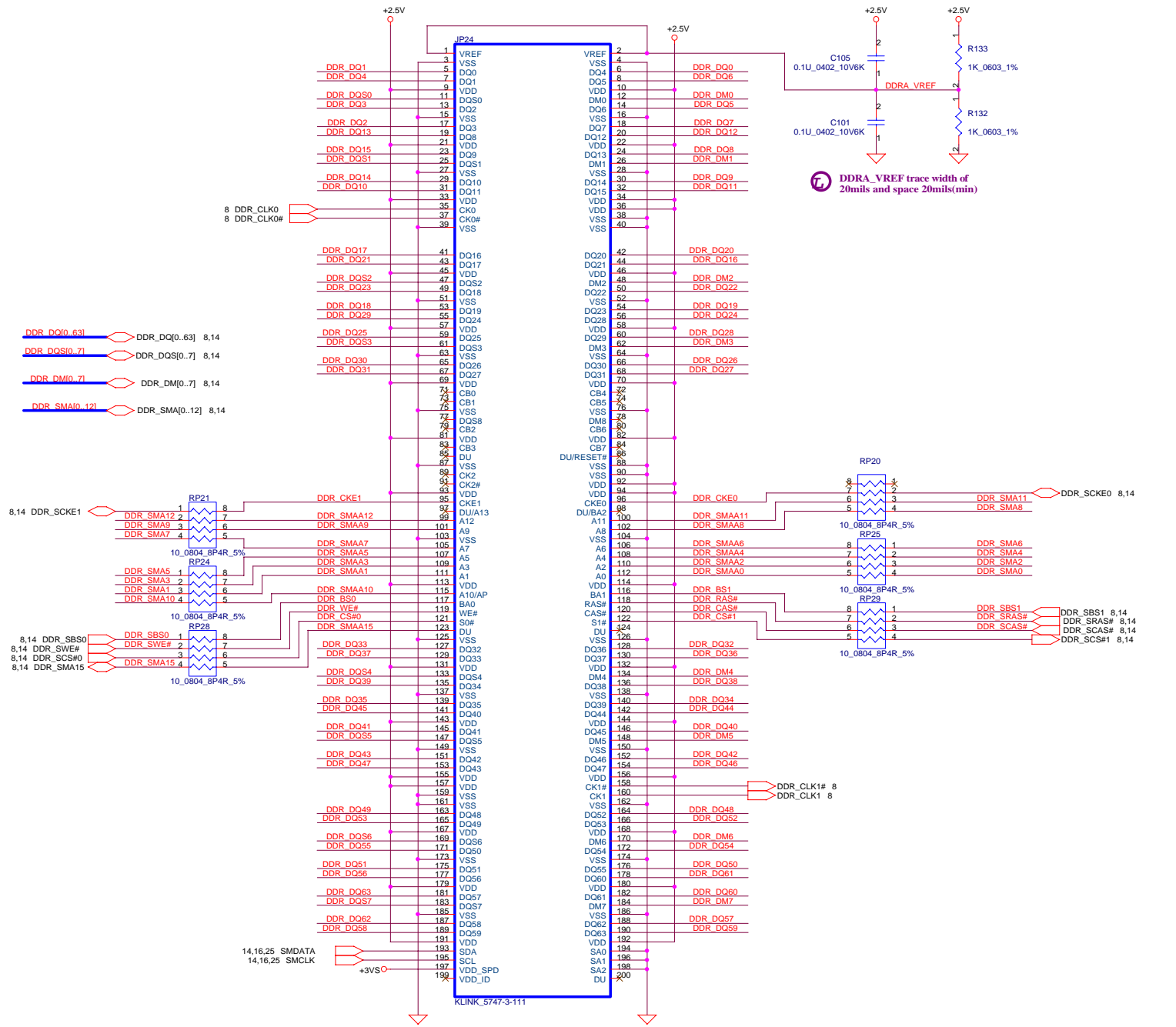
A_AD25/A_AD17 : CPU VOLTAGE[1..0]
DEFAULT: 0
 00: 1.05V
 01: 1.35V
 11: 1.75V
 10: 1.45V



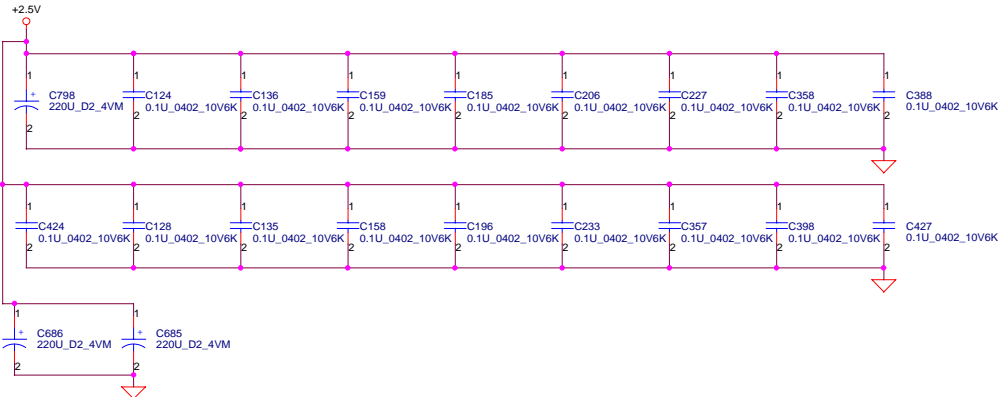
PAR: EXTENDED DEBUG MODE
DEFAULT: 1
 0: DEBUG MODE
 1: NORMAL

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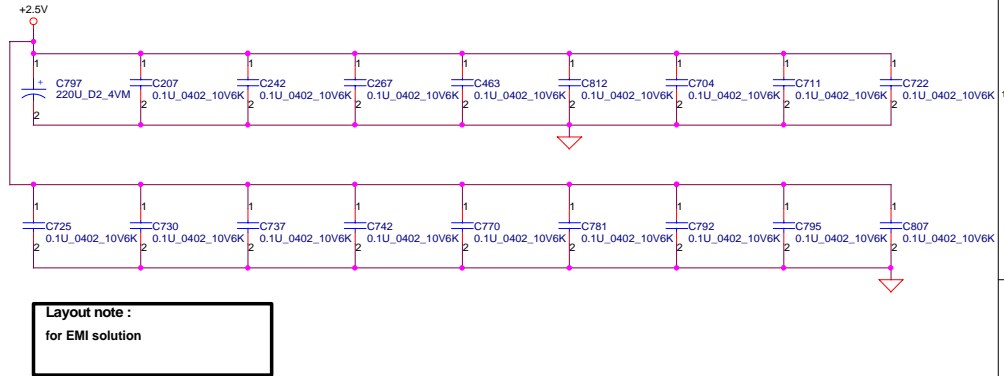
Compal Electronics, Inc.		
Title ATI RC300M-SYSTEM STRAP		
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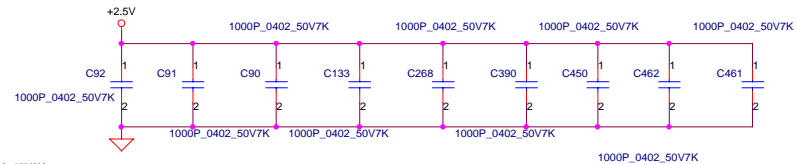
Layout note :
Distribute as close as possible to DDR-SODIMM0.



Layout note :
Distribute as close as possible to DDR-SODIMM1.



Layout note :
for EMI solution

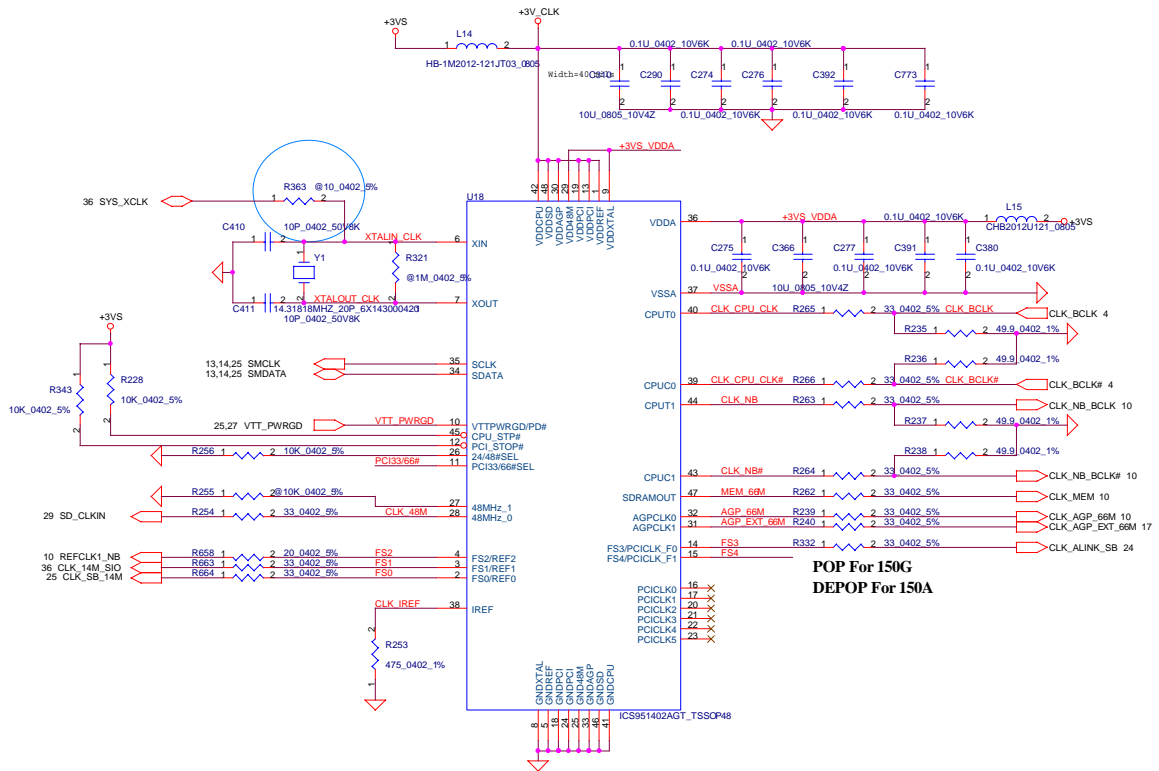


Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25VS



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Compal Electronics, Inc.		
Title DDR SODIMM Decoupling		
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POP For 150G
DEPOP For 150A

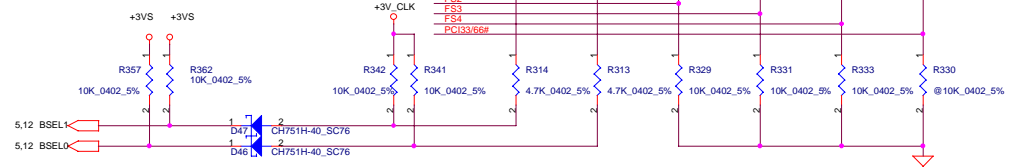
CLOCK FREQUENCY SELECT TABLE

FS4	FS3	FS2	FS1	FS0	CPU	MEM	With Spread Enabled...
0	0	0	1	0	200	200	Spread OFF OR Center spread +/-0.3%
0	0	0	0	1	133	133	
0	0	0	0	0	100	100	

A-LINK FREQ

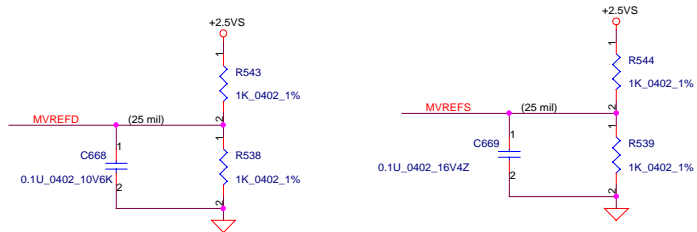
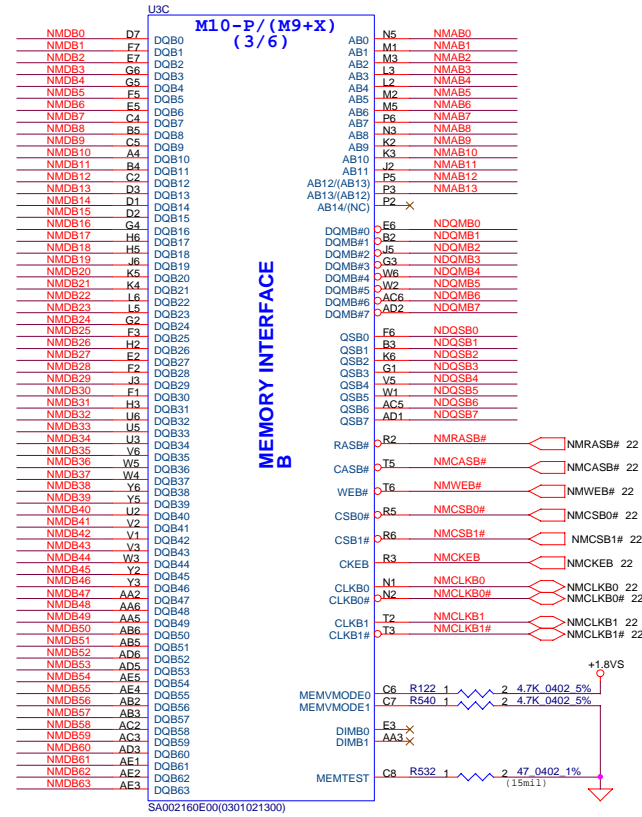
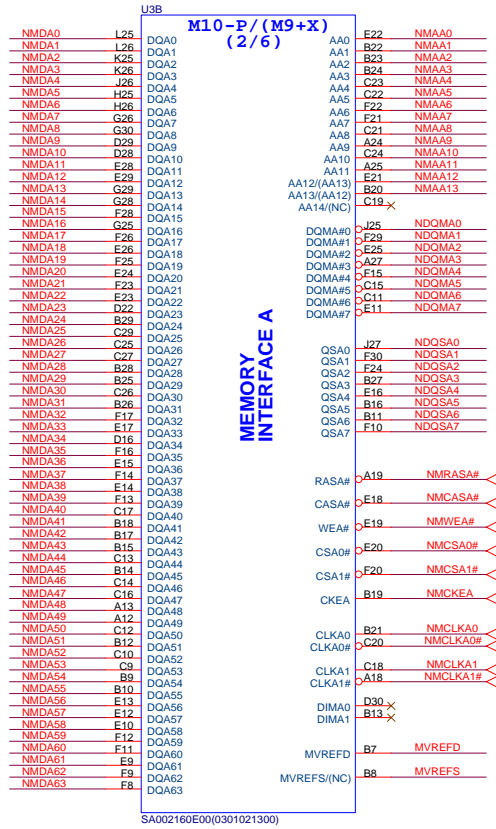
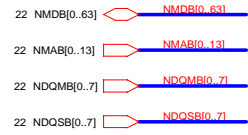
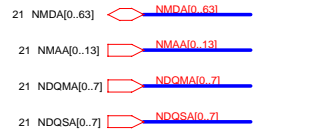
**	PC33/66# = HIGH	66MHZ
**	PC33/66# = LOW	33MHZ

Note: 0 = PULL LOW
1 = PULL HIGH



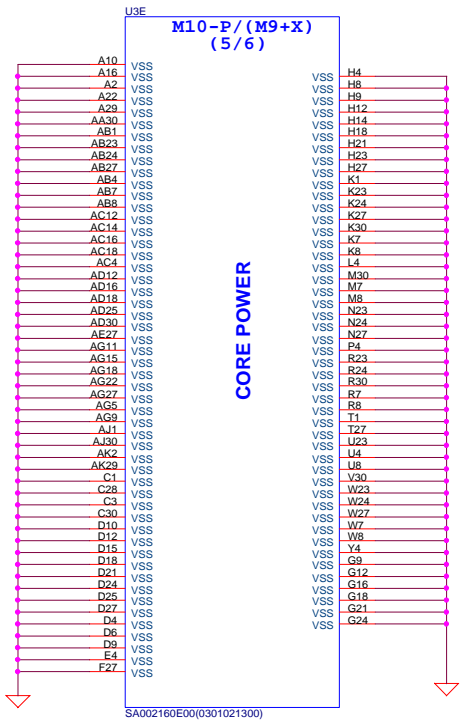
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MEMORY INTERFACE A

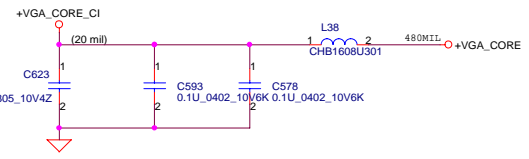
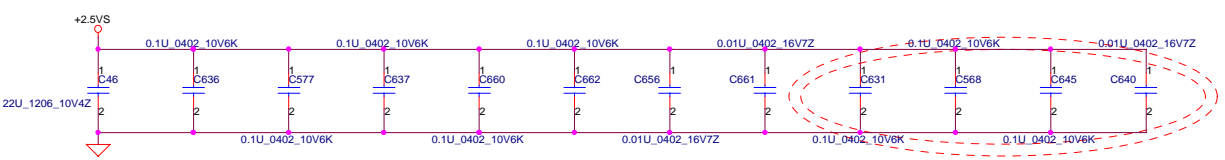
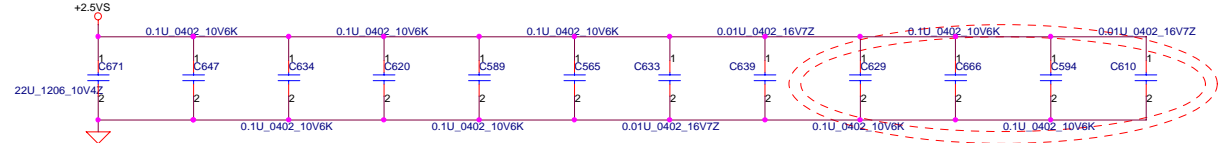
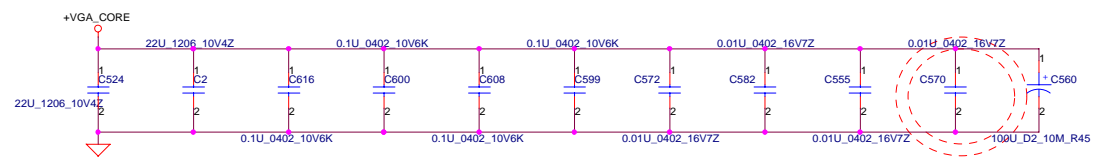
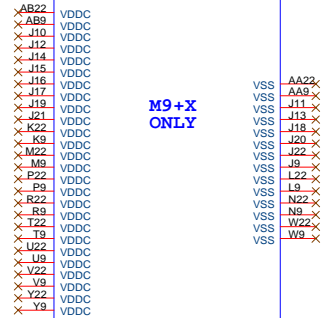
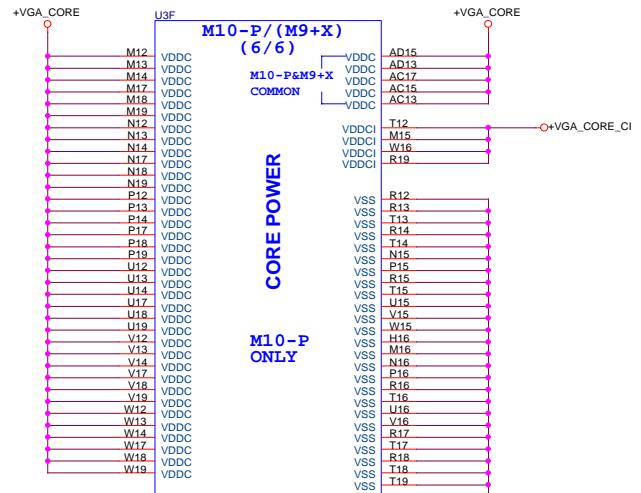


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Compal Electronics, Inc.		
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POWER INTERFACE



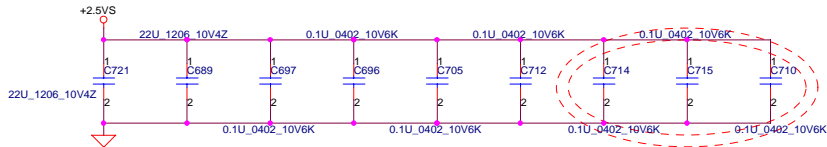
As close as possible to related pin

As close as possible to related pin

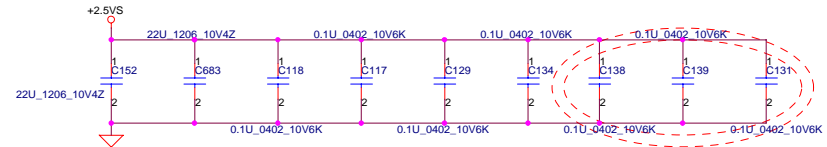
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Compal Electronics, Inc.		
Title ATI M10-P/M9+X POWER-B		
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VGA DDR FOR CHANNEL A

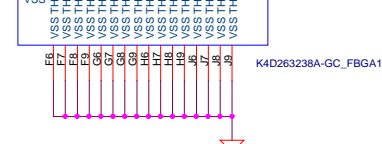
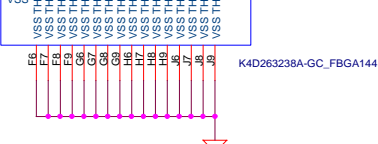
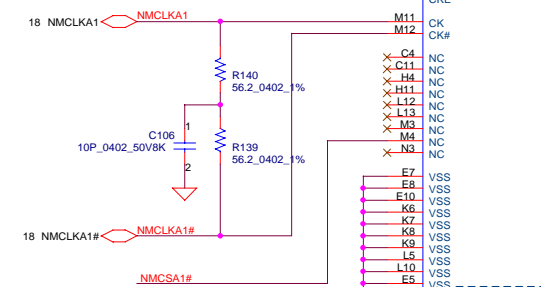
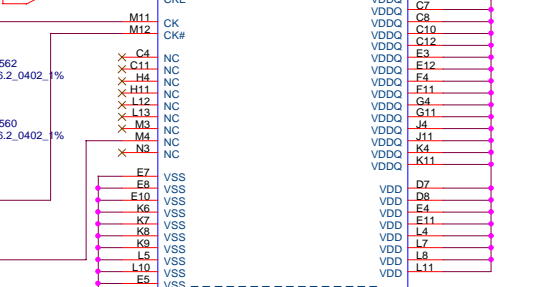
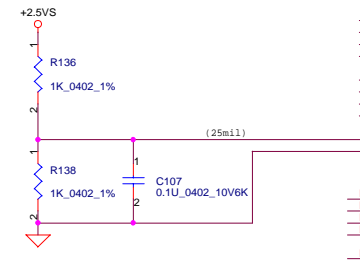
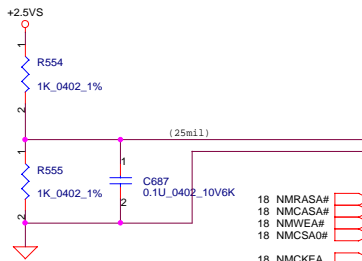
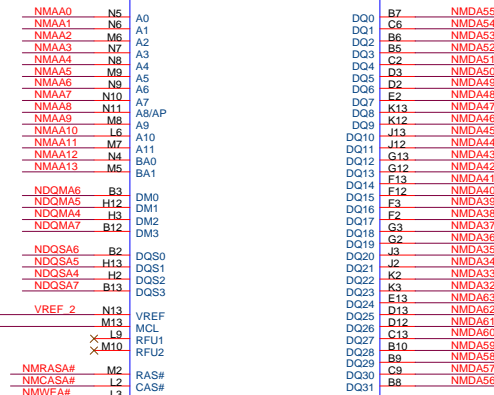
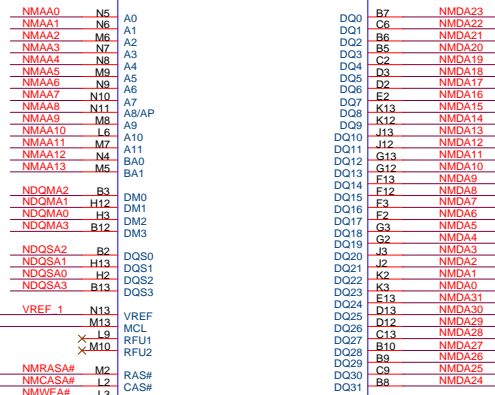
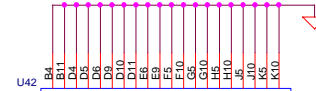
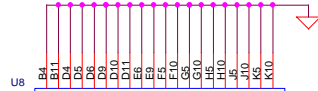


As close as possible to related pin



As close as possible to related pin

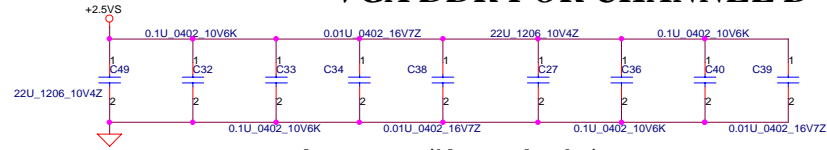
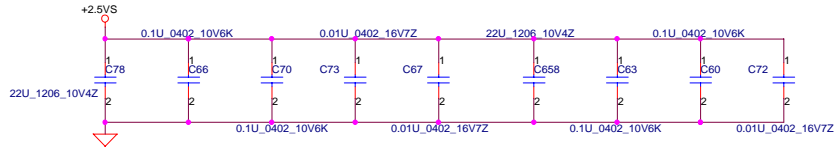
- 18 NMAA[0..13] \rightarrow NMAA[0..13]
- 18 NMDA[0..63] \rightarrow NMDA[0..63]
- 18 NDQMA[0..7] \rightarrow NDQMA[0..7]
- 18 NDQSA[0..7] \rightarrow NDQSA[0..7]



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Compal Electronics, Inc.		
VGA DDR FOR CHANNEL A		
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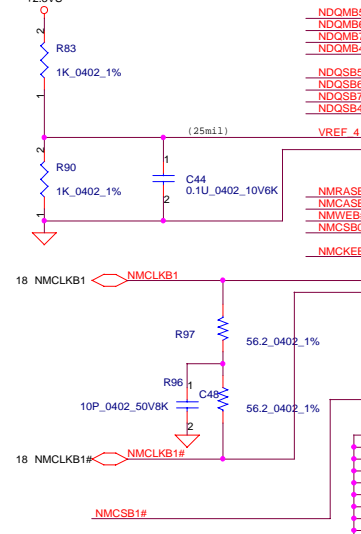
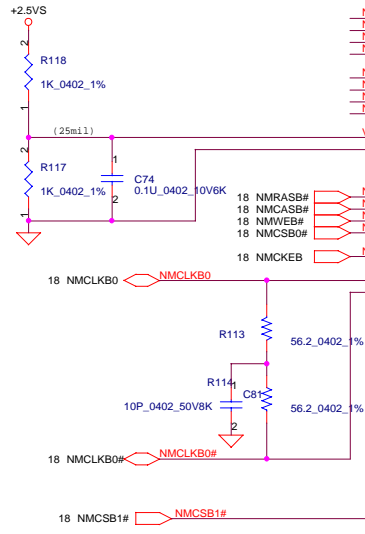
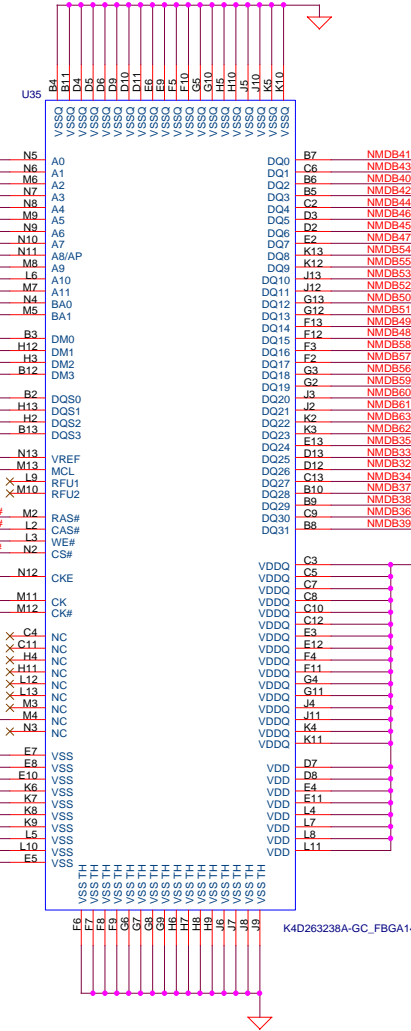
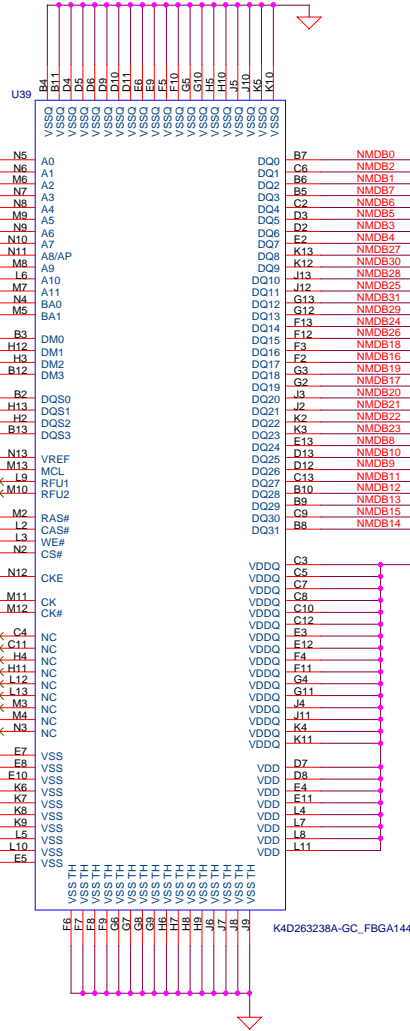
VGA DDR FOR CHANNEL B



As close as possible to related pin

As close as possible to related pin

- 18 NMAB[0..13] NMAB0..13
- 18 NMDB[0..63] NMDB0..63
- 18 NDQMB[0..7] NDQMB0..7
- 18 NDOSB[0..7] NDOSB0..7

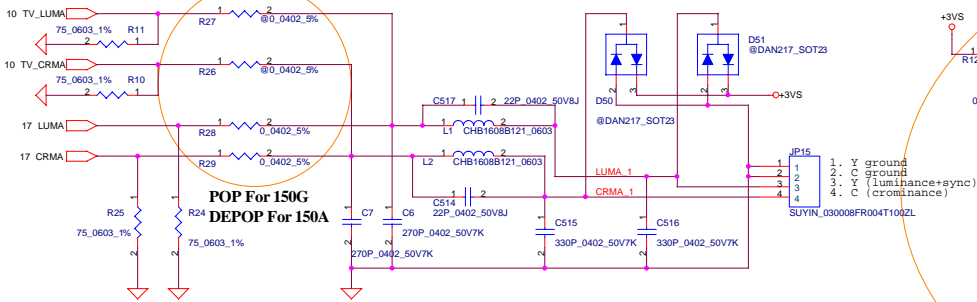


Compal Electronics, Inc.		
VGA DDR FOR CHANNEL B		
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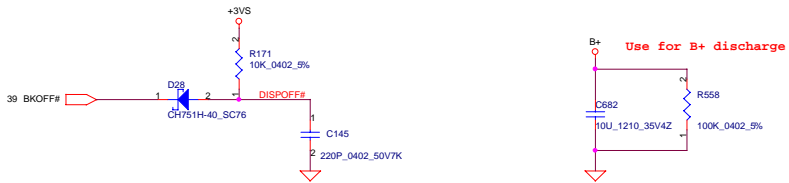
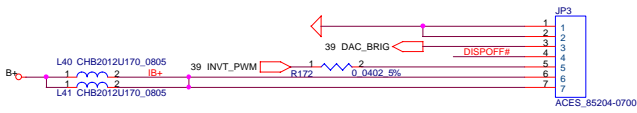
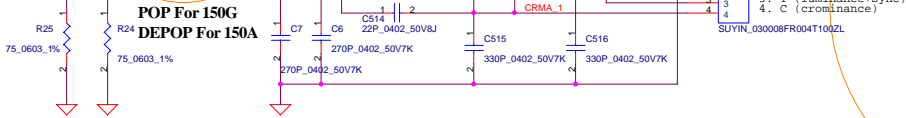
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**POP For 150A
DEPOP For 150G**

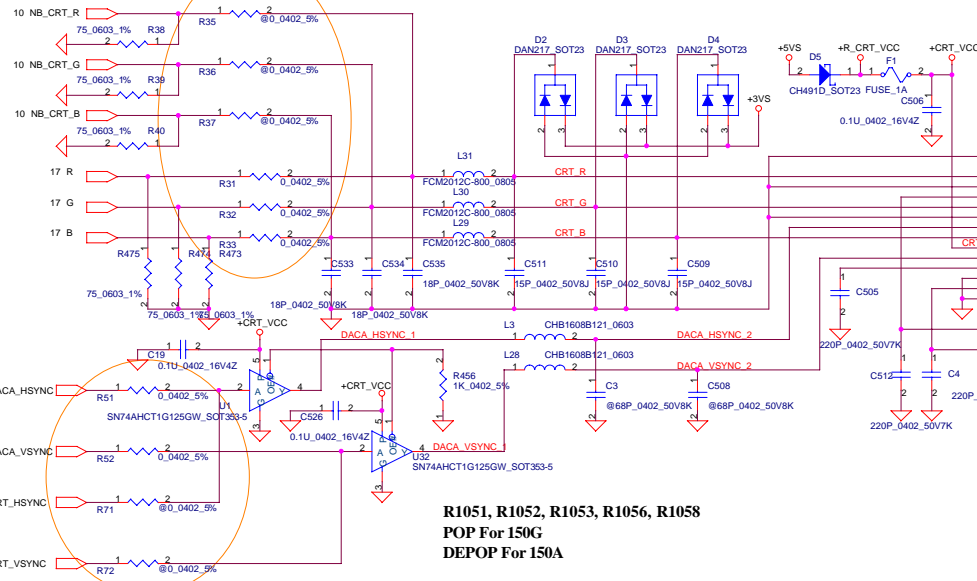
TV-OUT Conn.



**POP For 150G
DEPOP For 150A**



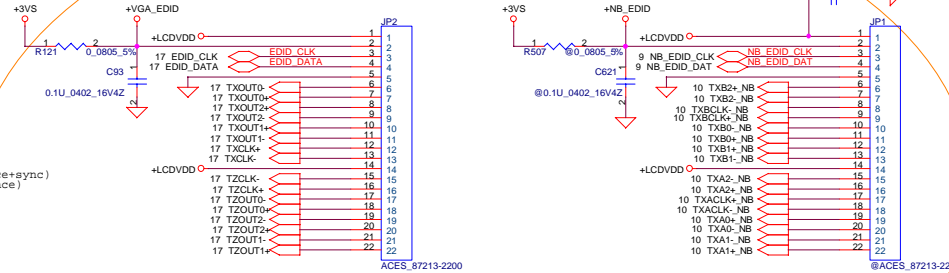
**R1045, R1047, R1049, R1060, R1061
POP For 150A
DEPOP For 150G**



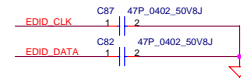
**R1051, R1052, R1053, R1056, R1058
POP For 150G
DEPOP For 150A**

LVDS Conn.

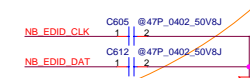
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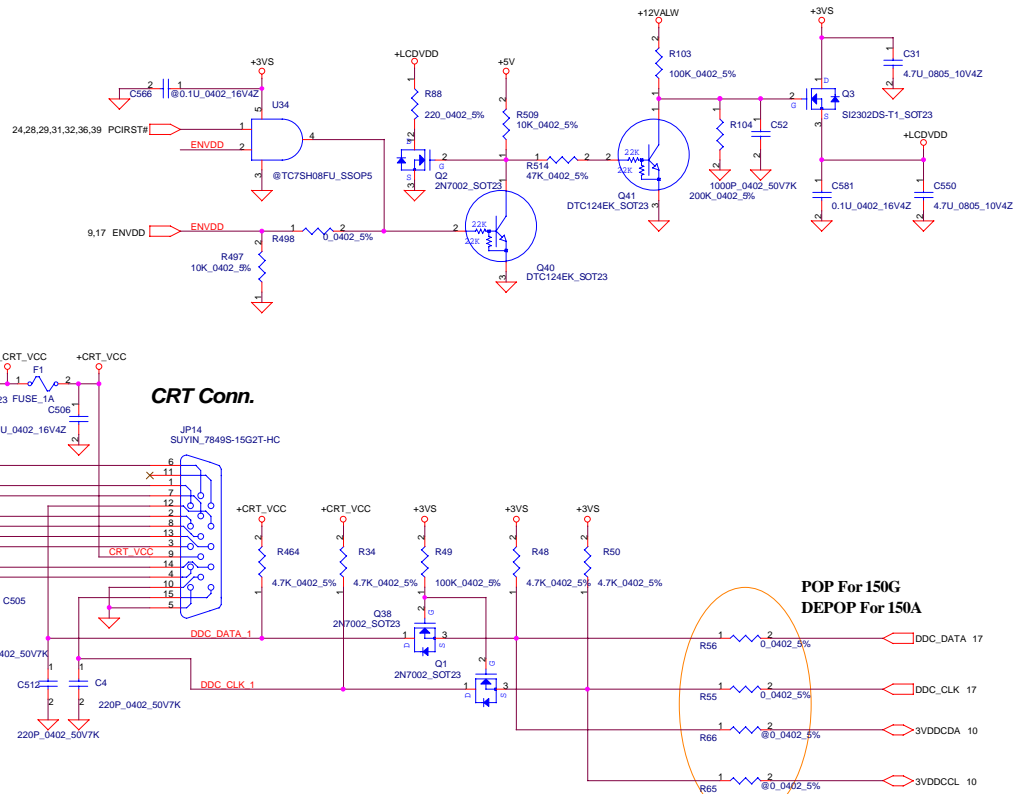
**POP For 150G
DEPOP For 150A**



**POP For 150A
DEPOP For 150G**



CRT Conn.



**POP For 150A
DEPOP For 150G**

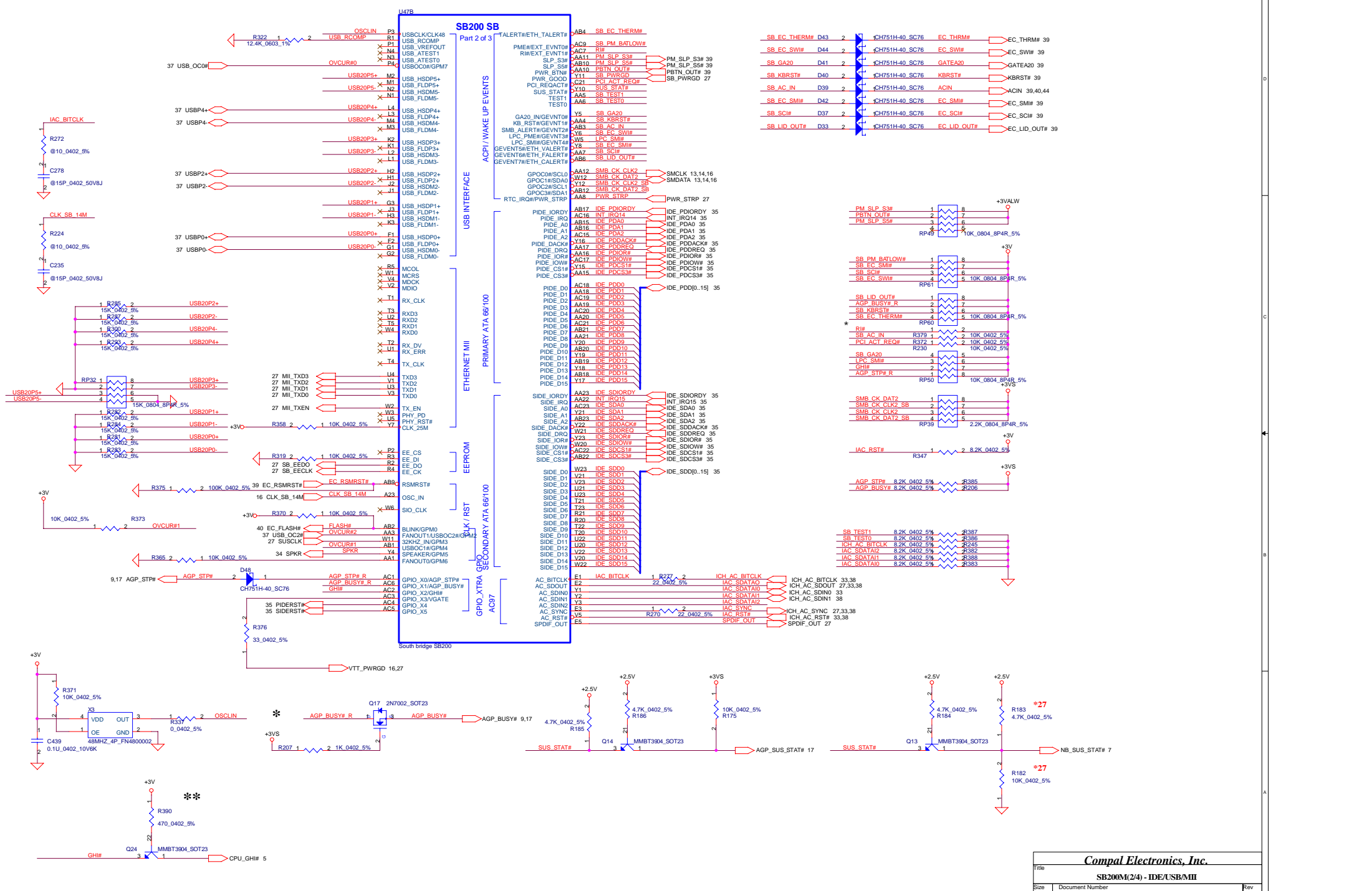
**POP For 150G
DEPOP For 150A**

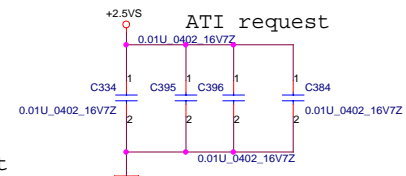
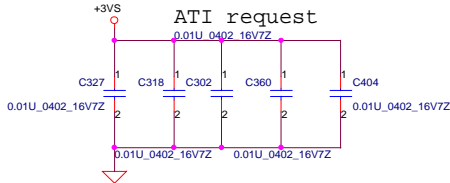
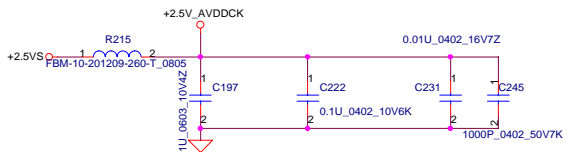
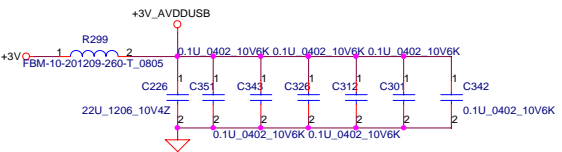
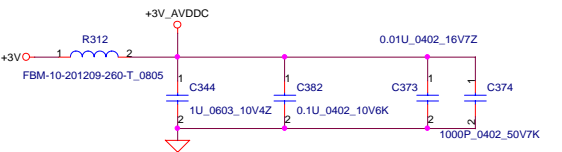
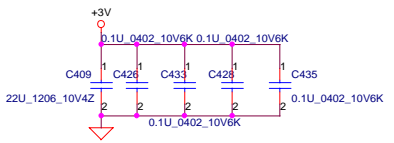
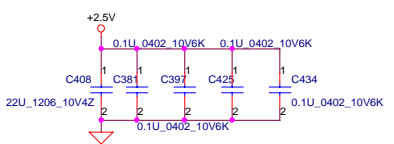
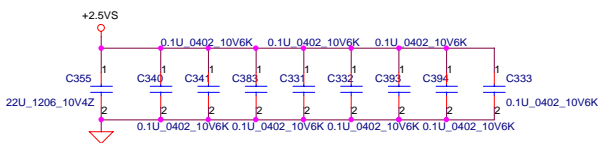
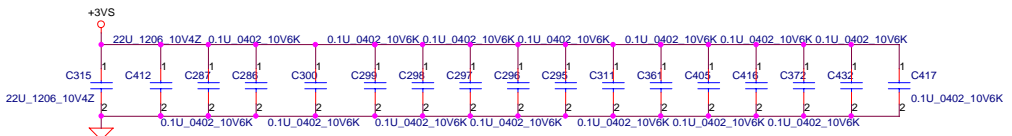
Compal Electronics, Inc.

CRT,TV-OUT & LVDS Connector

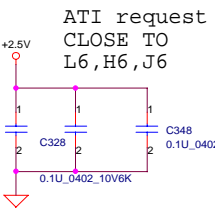
File	C Document Number		Rev
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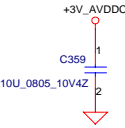




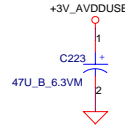
ATI request



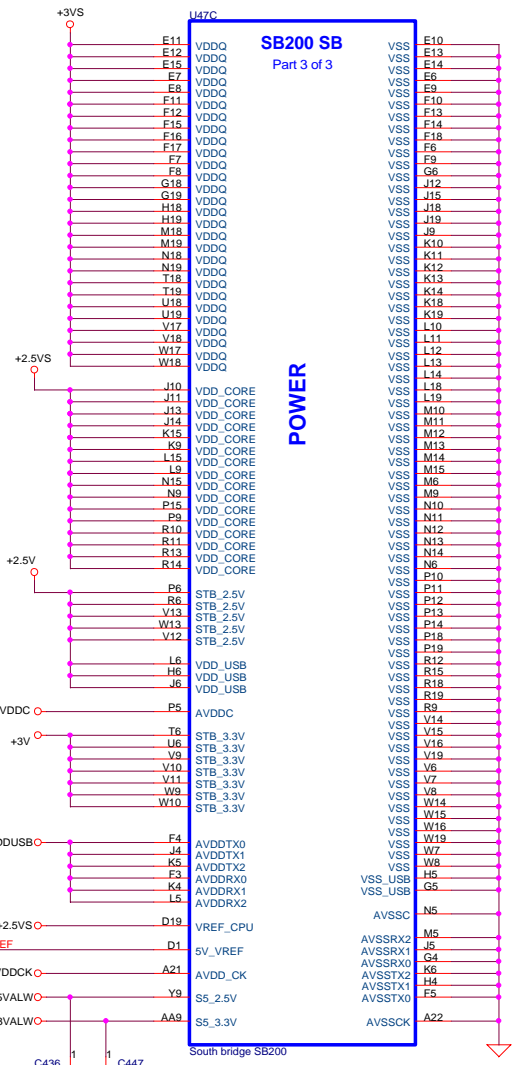
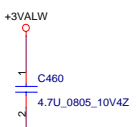
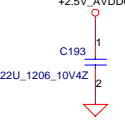
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ATI request

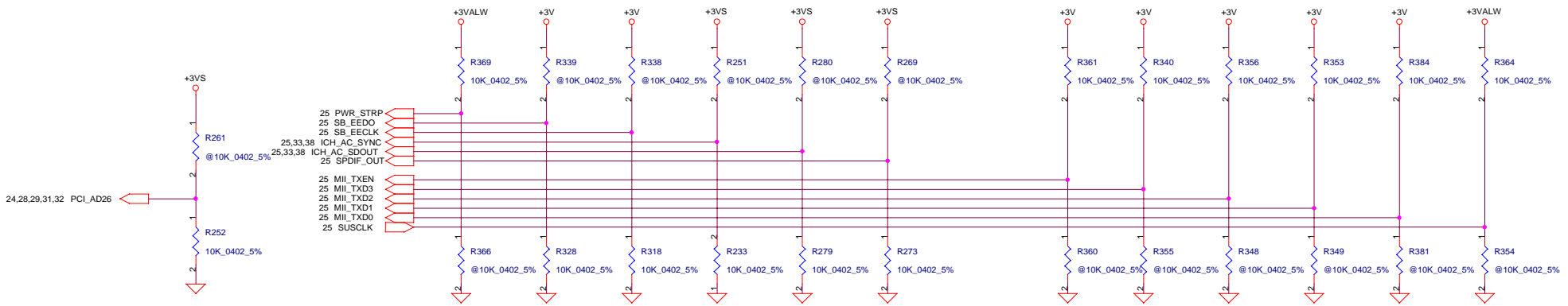


ATI request



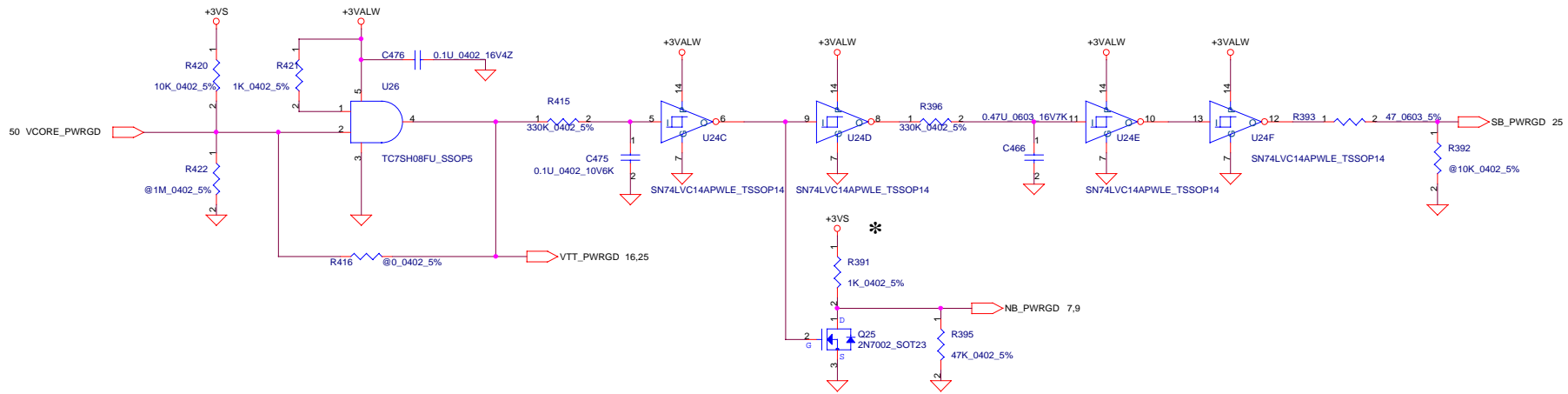
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Compal Electronics, Inc.		
SB200M(3/4) - PWR		
Title	Document Number	Rev
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REQUIRED SYSTEM STRAPS

	PWR_STRP	IGN DEBUG EEDO	EECK	AC_SYNC	AC_SDOUT	SPDIF_OUT	SPEEDSTEP CPU_STP#	FREQLTCH TX_EN	ETHERNET TXD[3:0]	32KHZ_S5
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	ROM ON PCI BUS	INIT ACTIVE HIGH	33MHz NB BUS	SIO 24MHz	ENABLE SPEED STEP	DISABLE CPU FREQ SETTING DEFAULT	PROCESSOR FREQ MULTIPLIER	32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (PII) DEFAULT	HI SPEED A-LINK DEFAULT	SIO 48MHz DEFAULT	DISABLE SPEED STEP DEFAULT	ENABLE CPU FREQSETTING		32KHZ INPUT TO SB200 (EXT RTC)



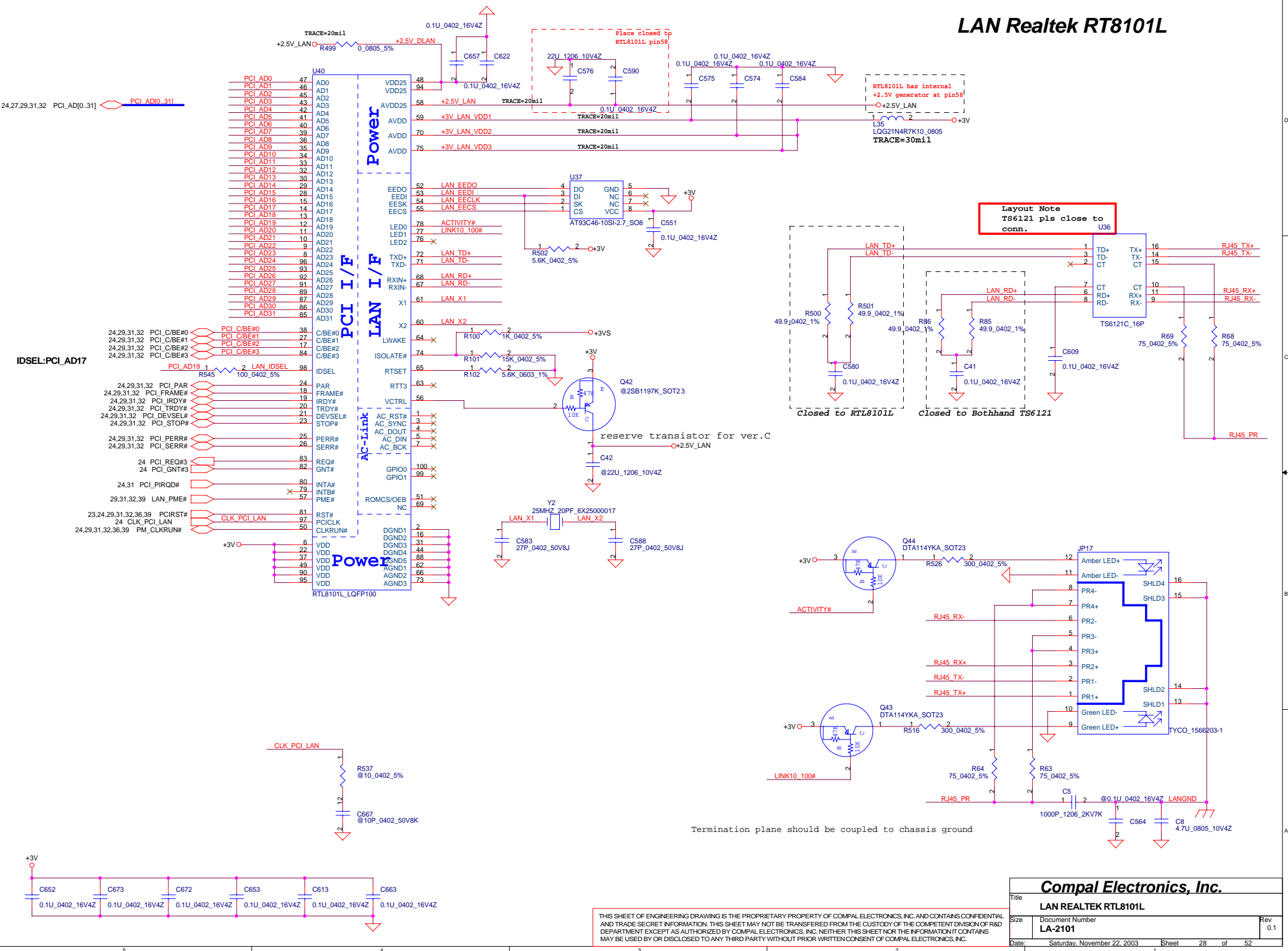
Compal Electronics, Inc.

SB200M(4/4) - STRAPS

Title		
Size	Document Number	Rev
	LA-2101	0.1
Date	Saturday, November 22, 2003	Sheet 27 of 52

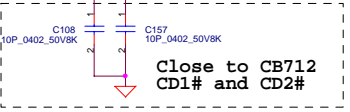
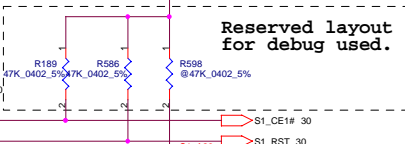
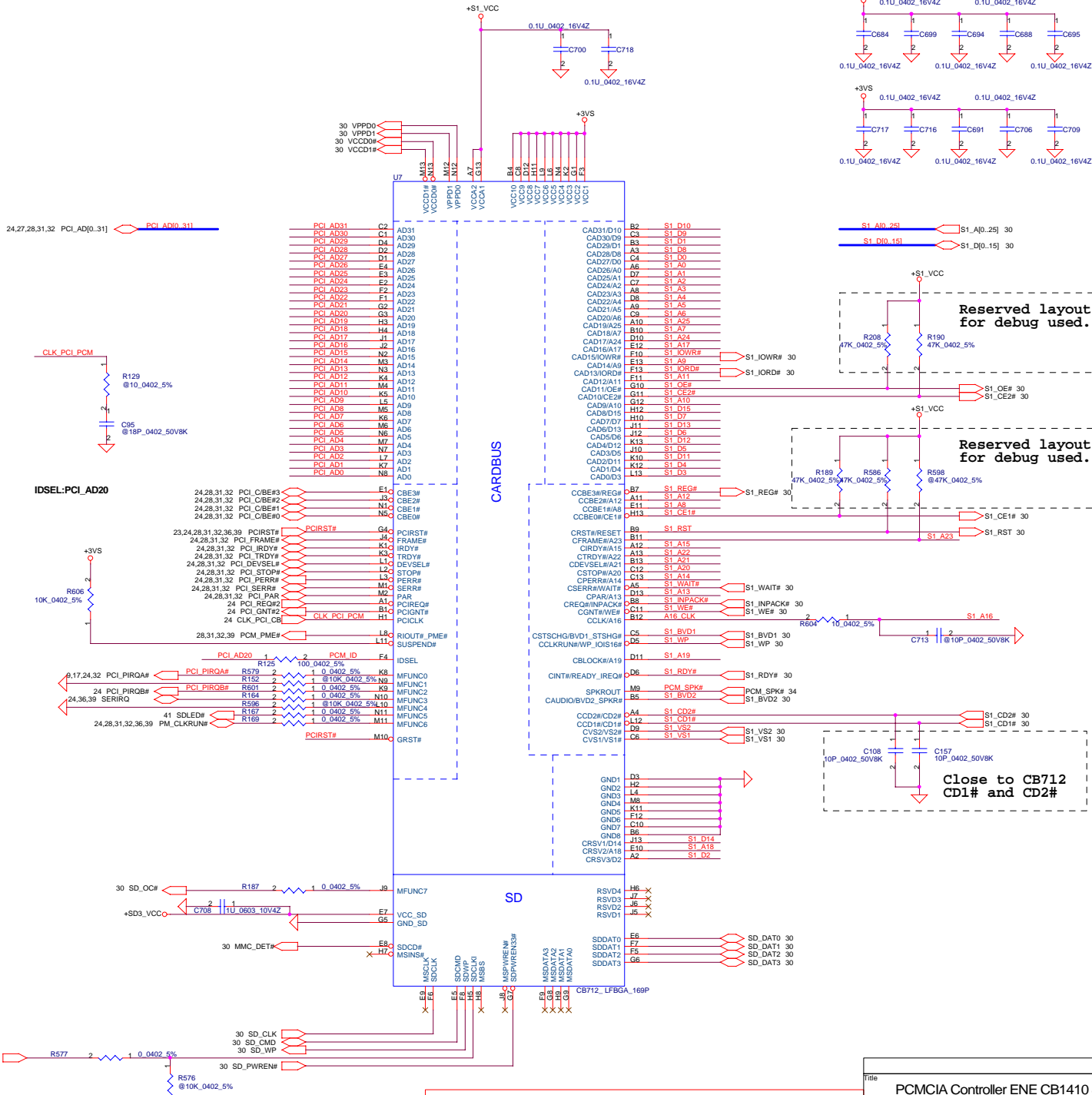
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LAN Realtek RT8101L



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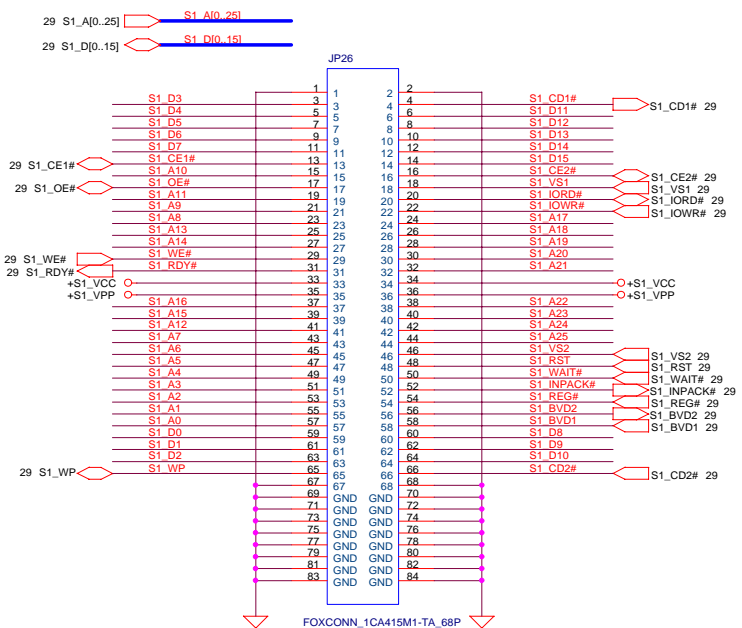
Compal Electronics, Inc.		
Title	LAN REALTEK RTL8101L	
Size	Document Number	Rev
	LA-2101	0.1
Date	Saturday, November 22, 2003	Sheet 28 of 52



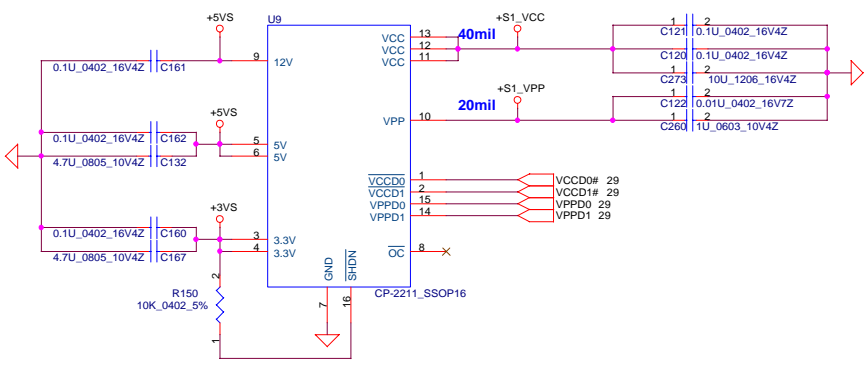
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Title		PCMCIA Controller ENE CB1410 & CB712	
Size	Document Number	Rev	
Custom	LA-2101	0.1	
Date	Saturday, November 22, 2003	Sheet	29 of 52

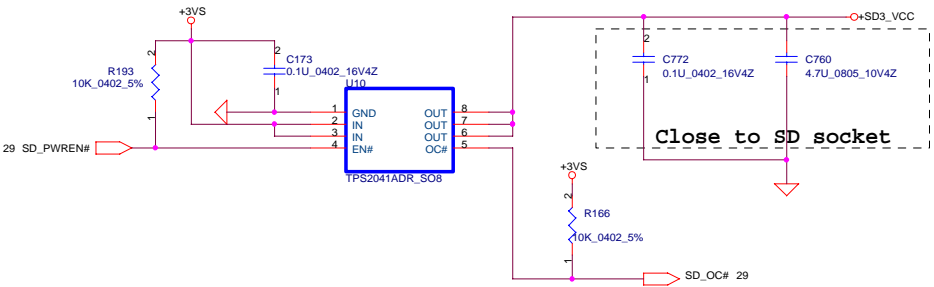
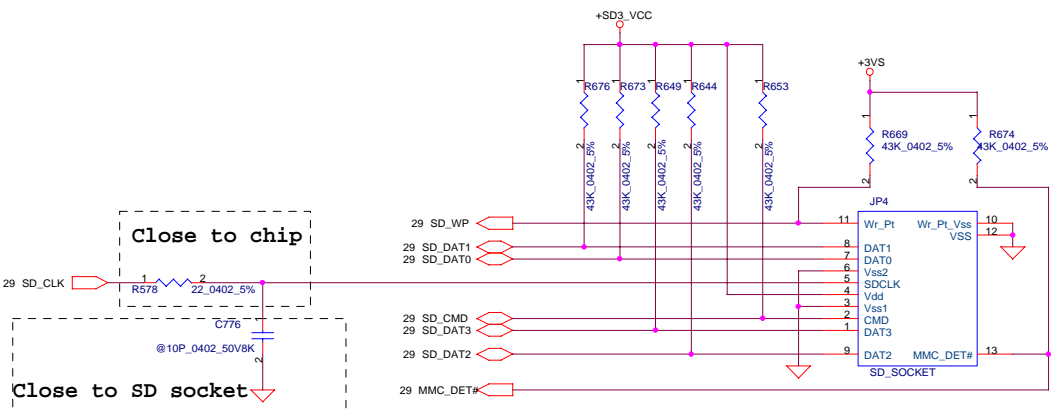
CARDBUS SOCKET



PCMCIA Power Controller

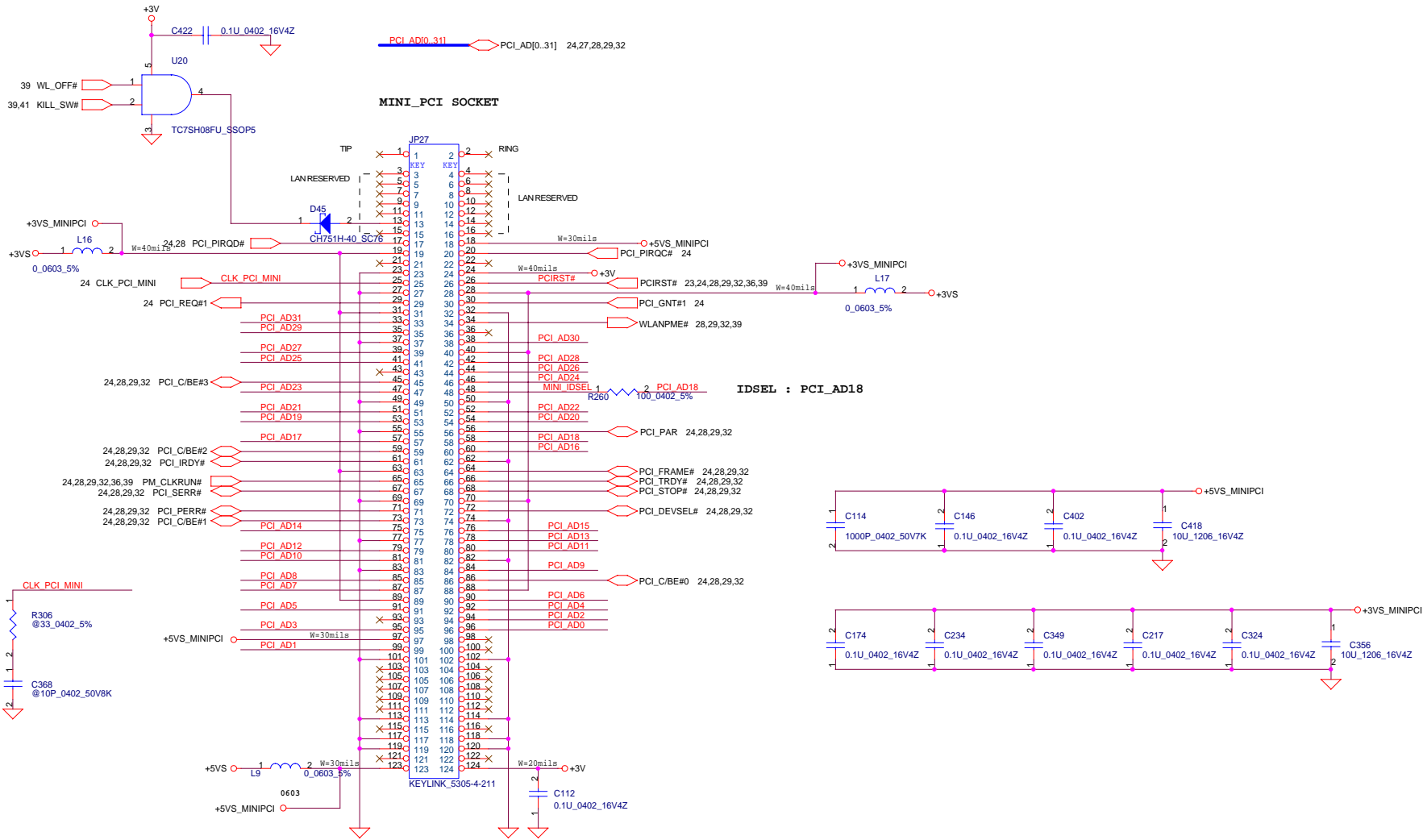


SD SOCKET



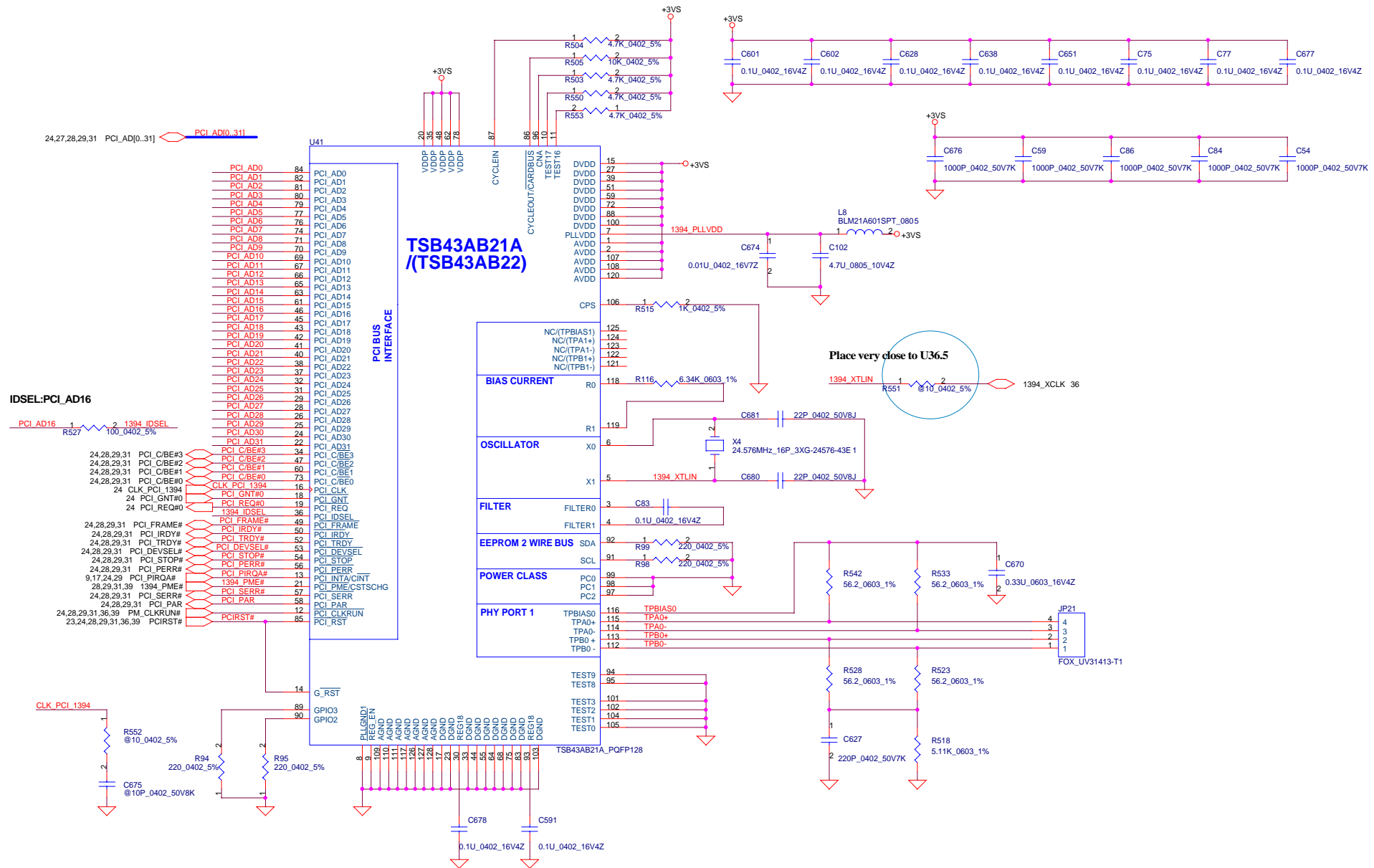
Compal Electronics, Inc.		
Title	PCMCIA/SD SOCKET	
Size	Document Number	Rev
Customer	LA-2101	0.1
Date:	Saturday, November 22, 2003	Sheet 30 of 52

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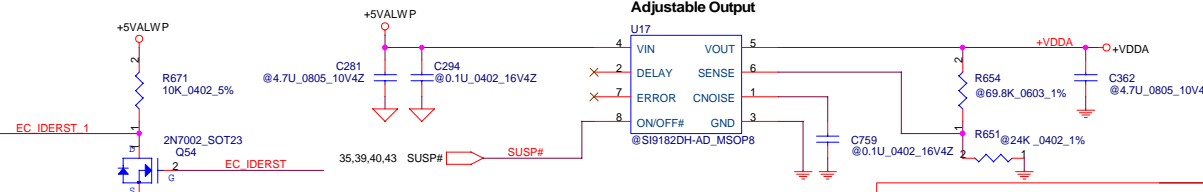
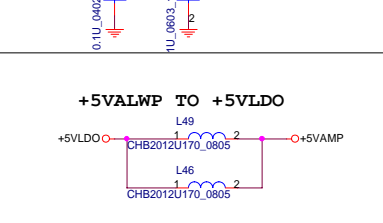
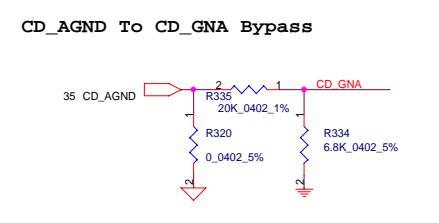
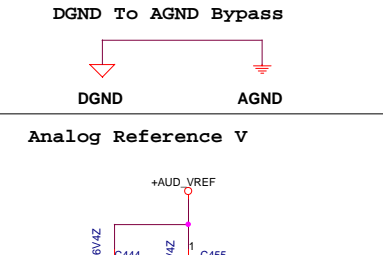
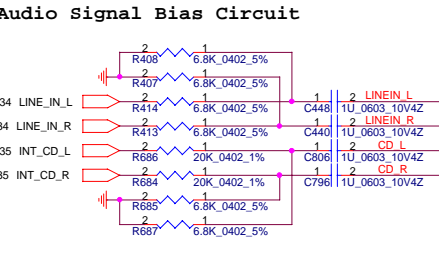
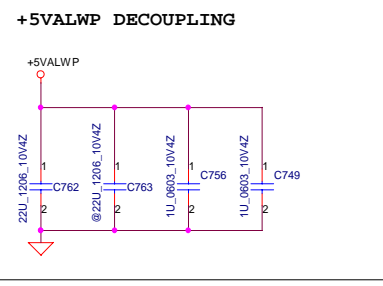
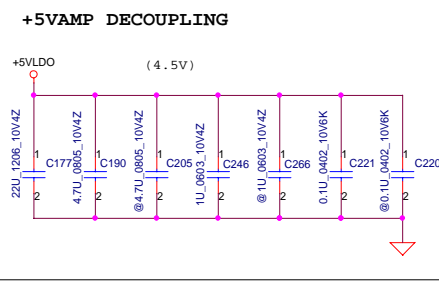
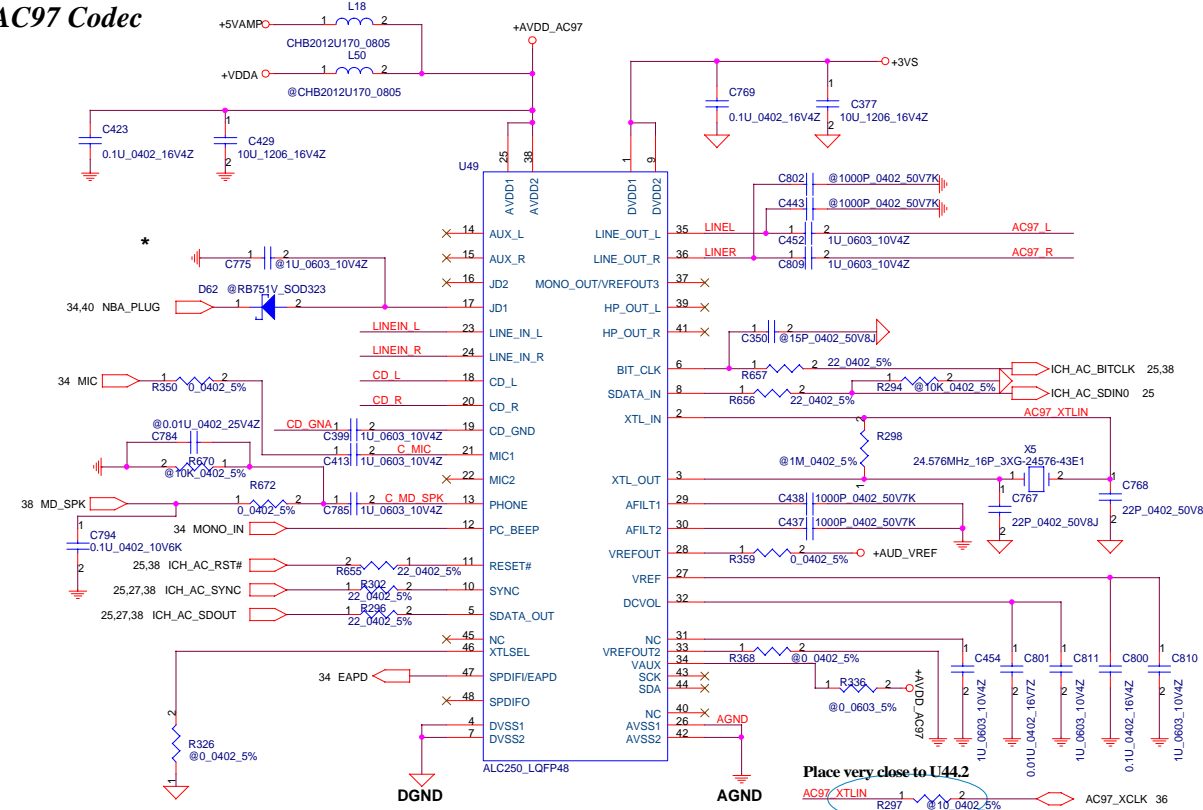
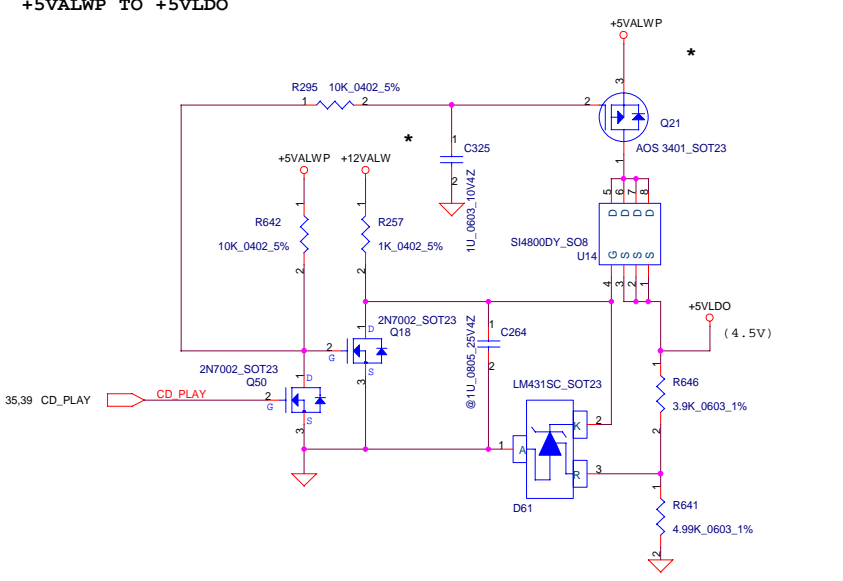
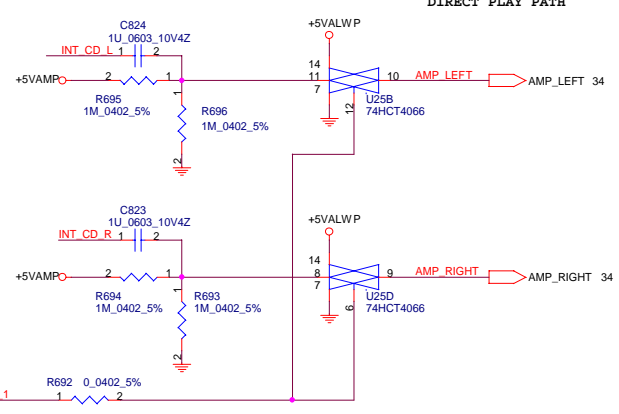
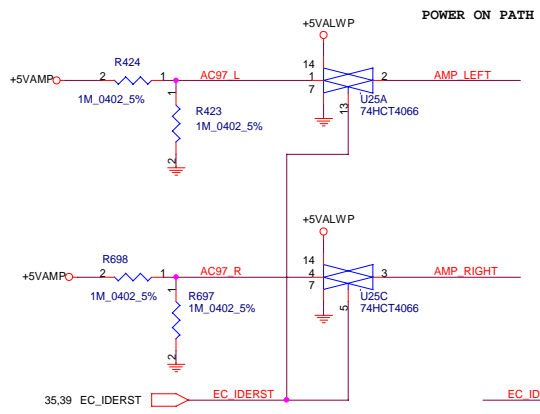
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Compal Electronics, Inc.		
Title		
MINI_PCI		
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Compal Electronics, Inc.		
Title	1394 Interface	
Size	Document Number	Rev
Customer	LA-2101	0.1
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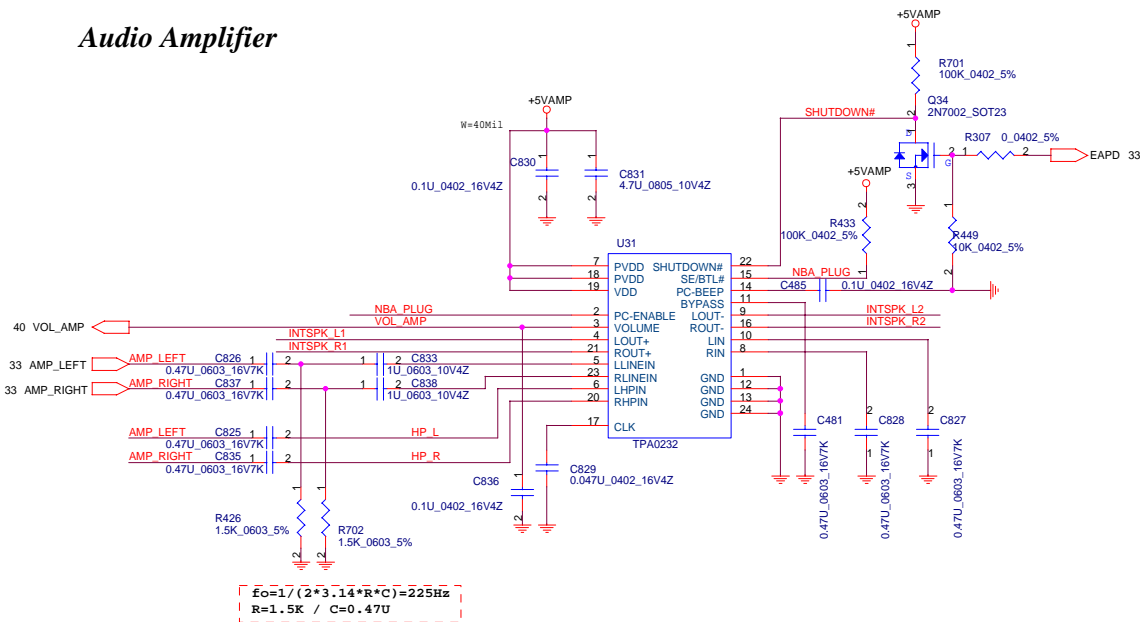
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Compal Electronics, Inc.		
Title	AC97 Codec	
Size	Document Number	Rev
Custom	LA-2101	0.1
Date	Saturday, November 22, 2003	Sheet 33 of 52

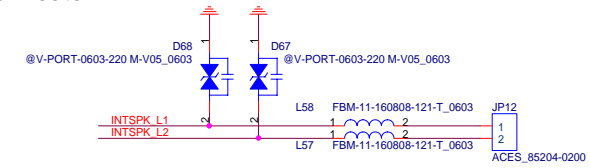
Audio Amplifier



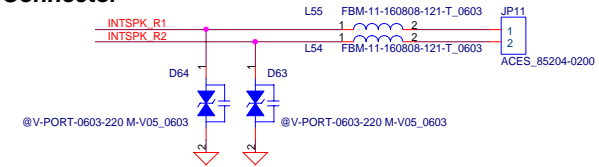
$$f_o = 1 / (2 * 3.14 * R * C) = 225\text{Hz}$$

R=1.5K / C=0.47U

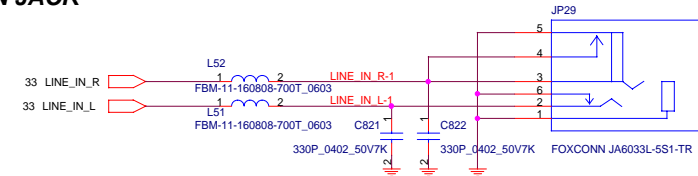
Left Speaker Connector



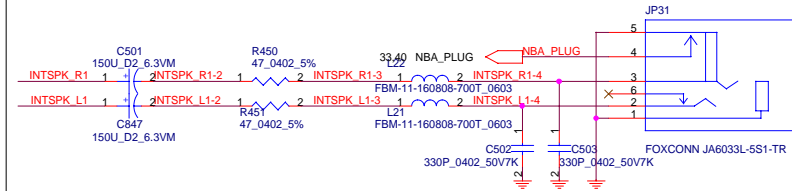
Right Speaker Connector



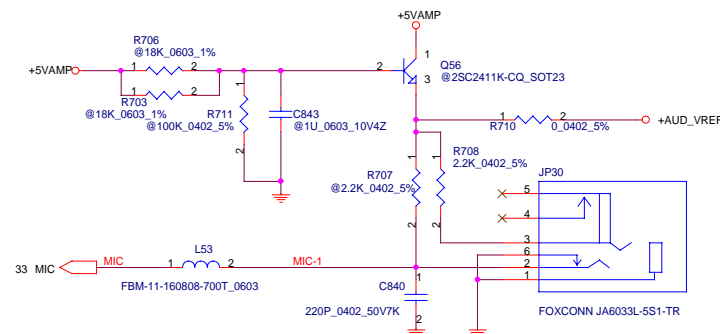
LINE IN JACK



HEADPHONE OUT JACK

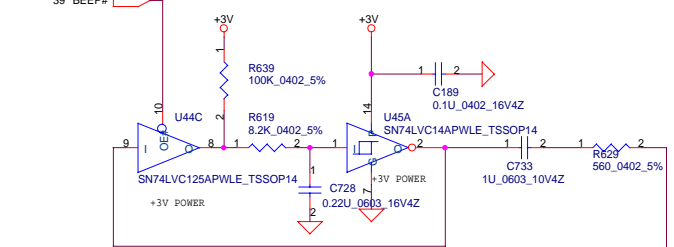


MICROPHONE IN JACK

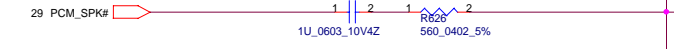


Compal Electronics, Inc.		
Title	AMP & Audio Jack	
Size	Document Number	Rev
Custom	LA-2101	0.1
Date	Saturday, November 22, 2003	Sheet 34 of 52

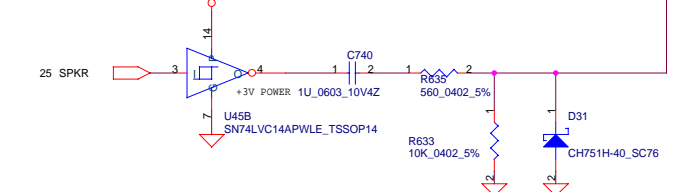
EC BEEP



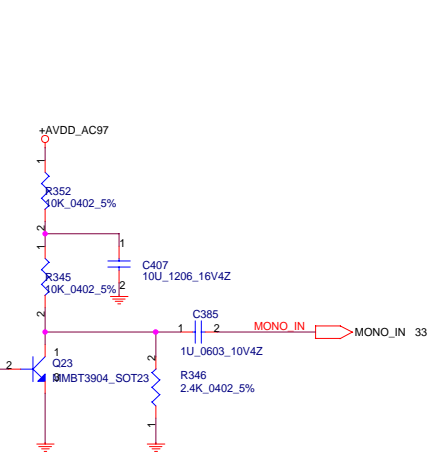
CardBus BEEP



PCI BEEP

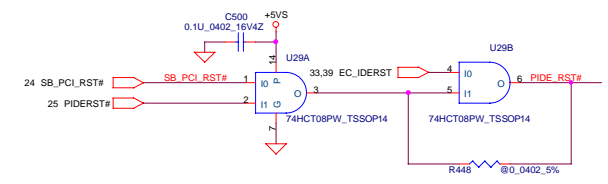
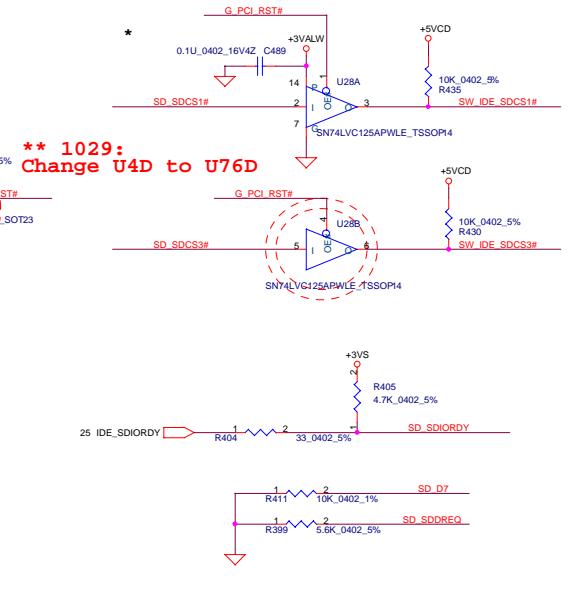
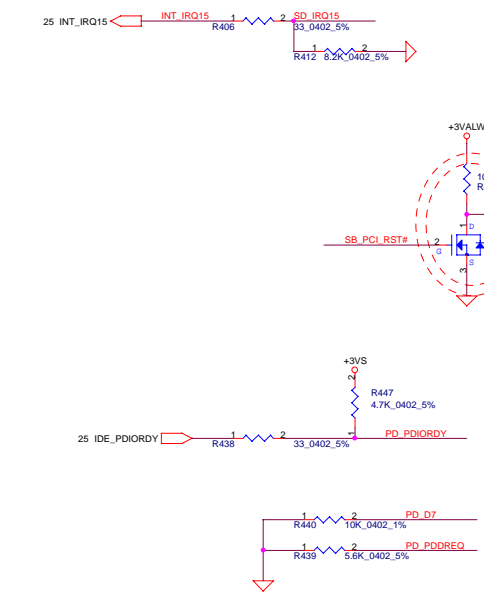
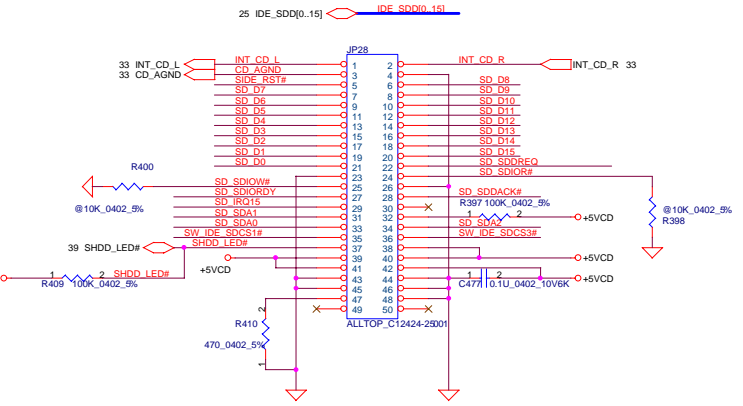
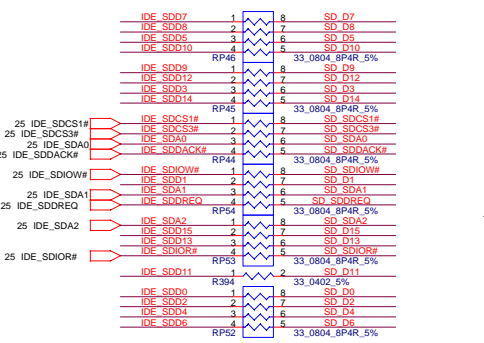
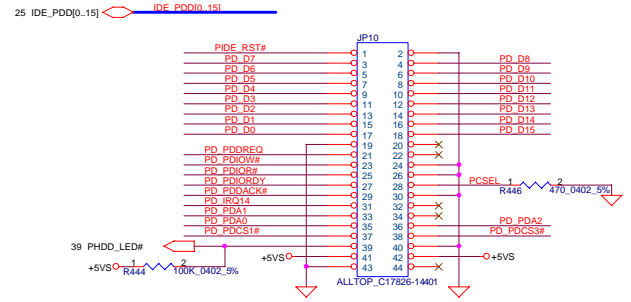
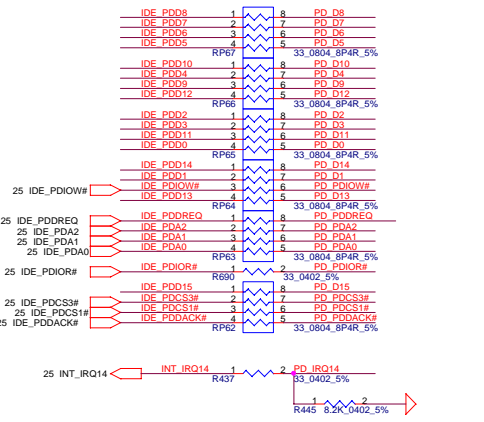


System BEEP To AC97' Codec

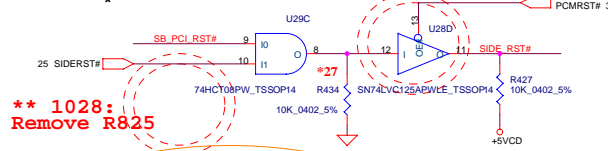


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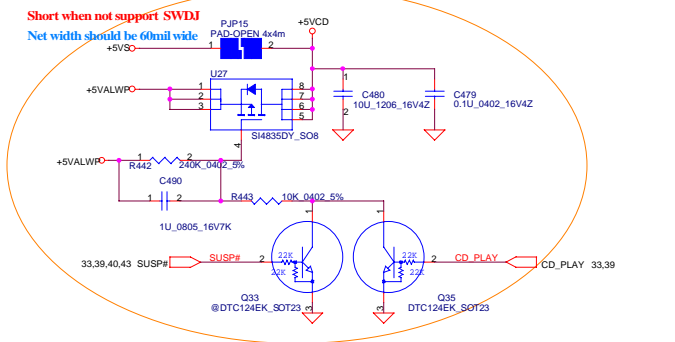
HDD CONNECTOR



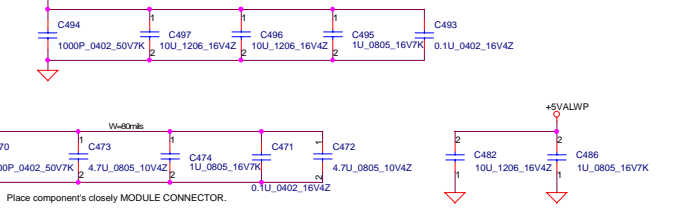
**** 1029: Change U4D to U76D**



**** 1028: Remove R825**

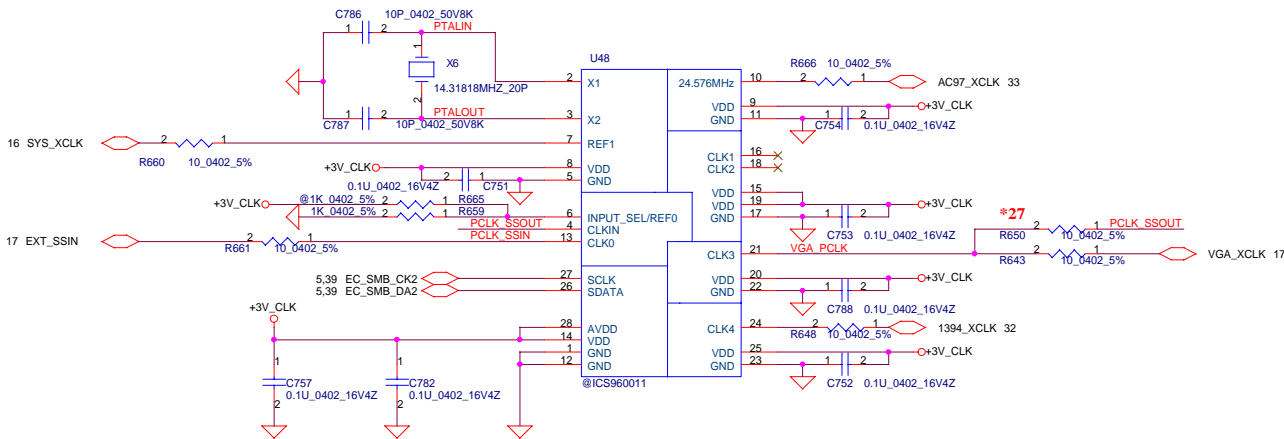
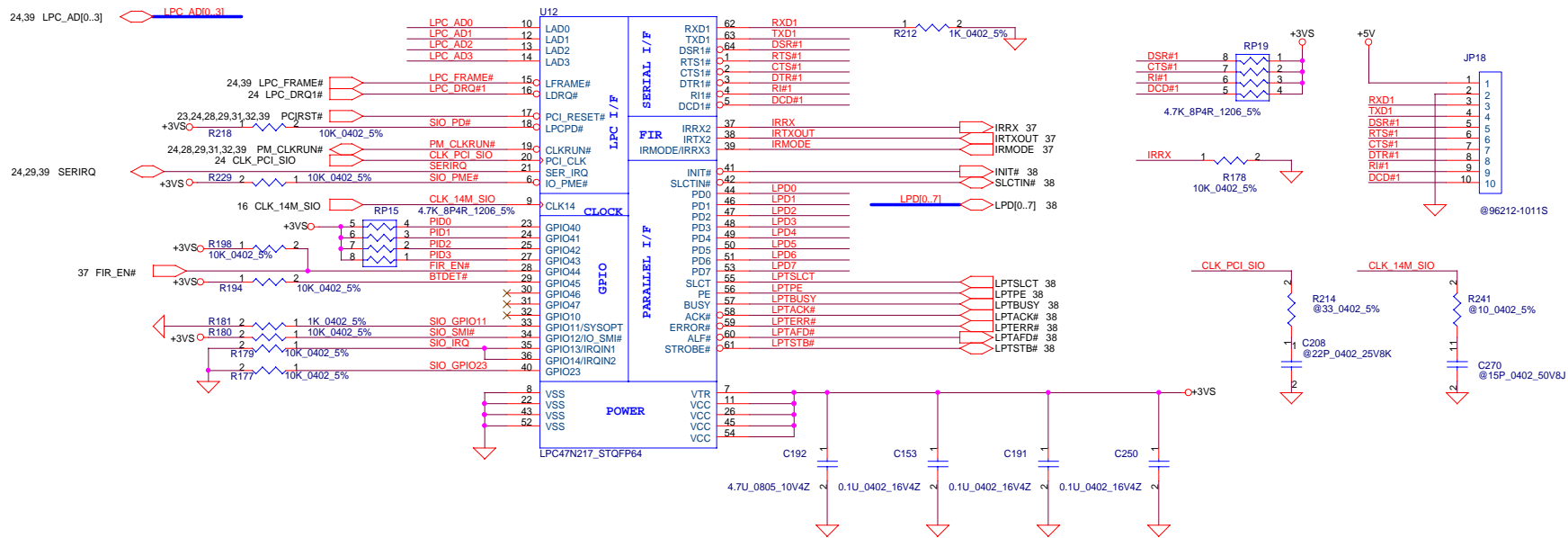


Place caps near HDD CONN.



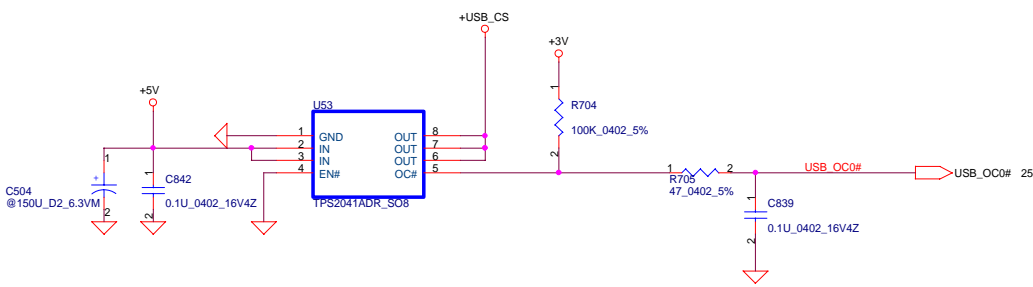
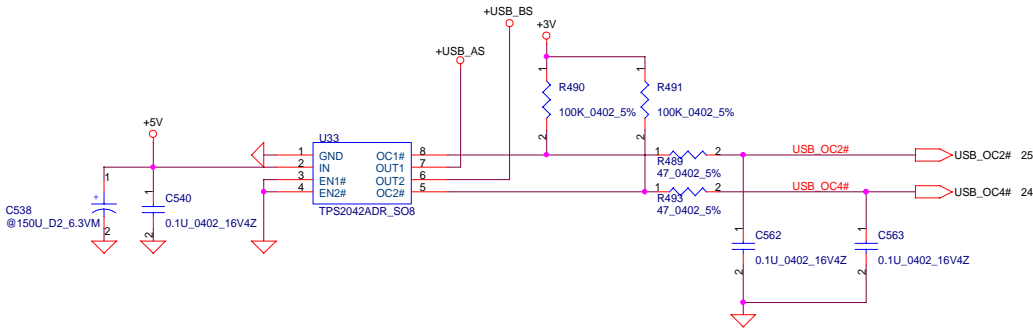
Compal Electronics, Inc.	
Title	IDE/FDD MODULE CONN.
Size	Document Number
C	LA-2101
Date:	Saturday, November 22, 2003
Sheet	35 of 52
Rev	0.1

SUPER I/O SMC FDC47N217

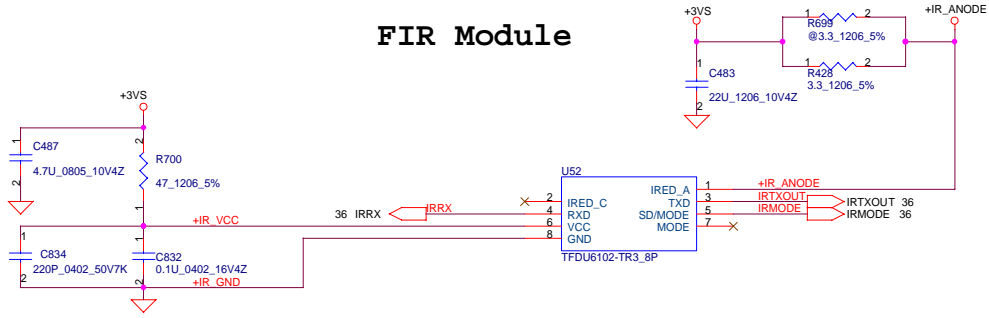


Compal Electronics, Inc.		
Title		
SUPER I/O		
Size	Document Number	Rev
Custom	LA-2101	0.1
Date:	Saturday, November 22, 2003	Sheet 36 of 52

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FIR Module



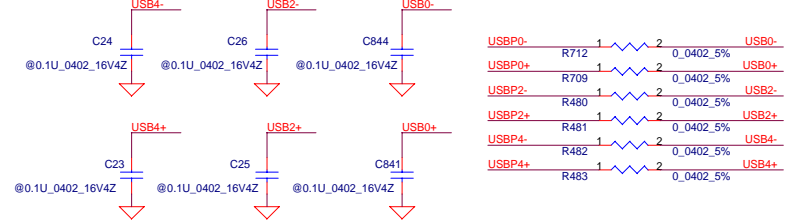
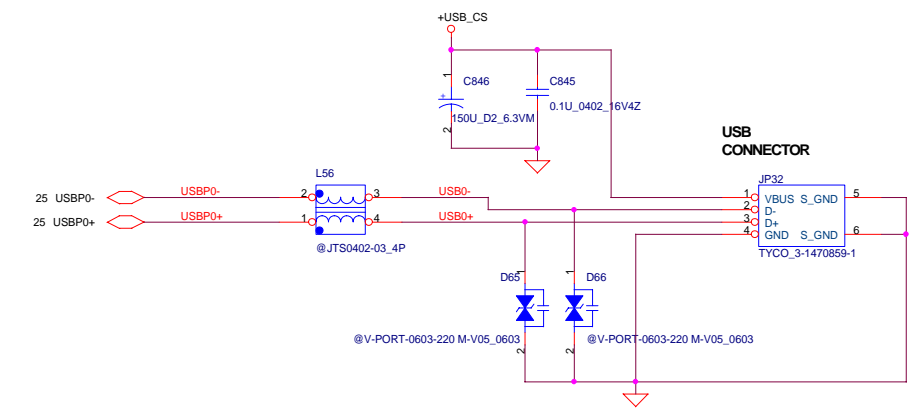
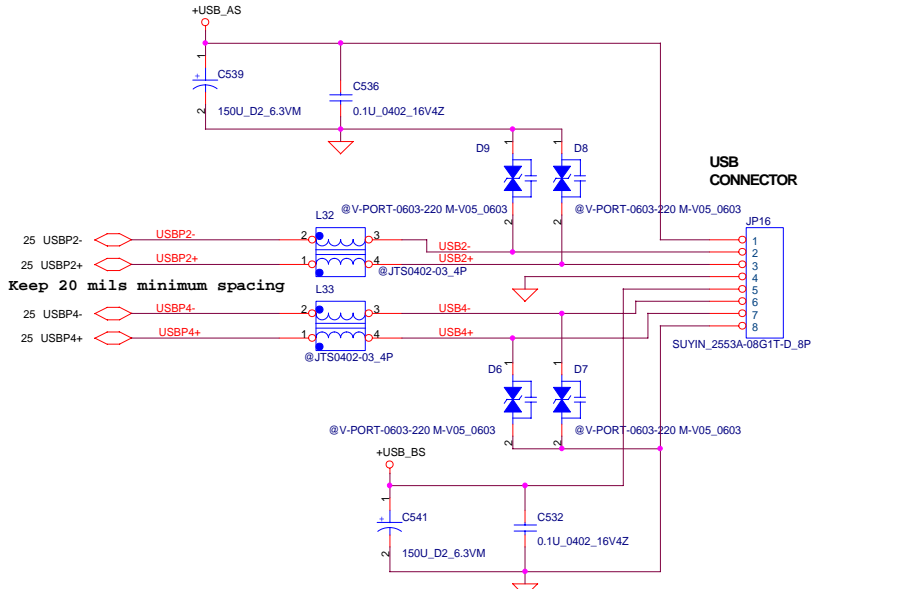
36 FIR_EN#

FIR_EN#

LOW FIR Poped

HIGH FIR Un-Poped

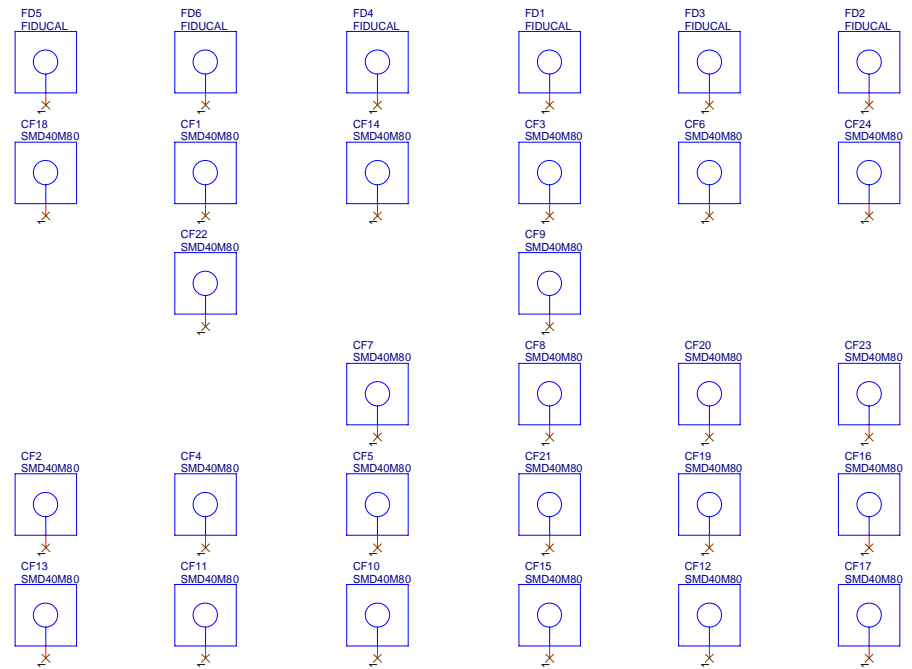
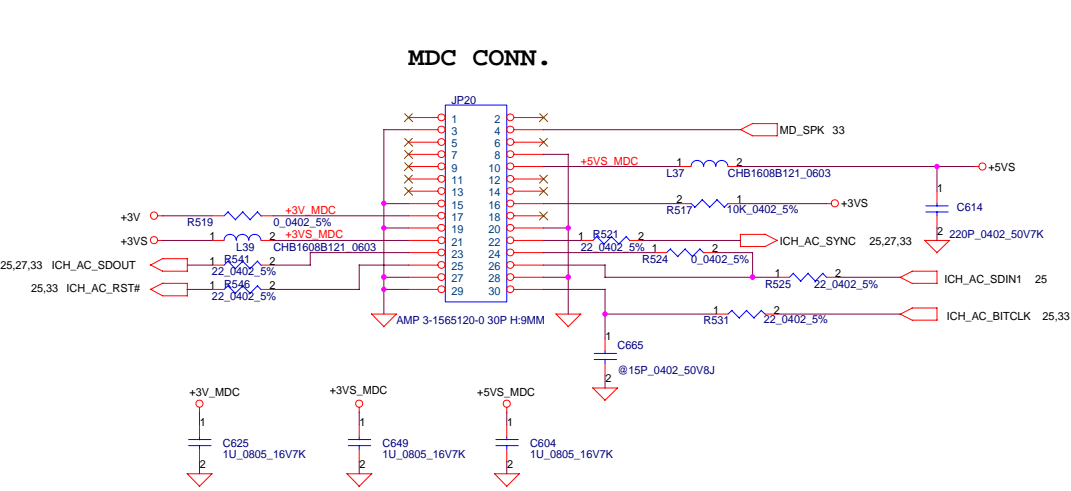
The component's most place cloely IRDA MODULE.



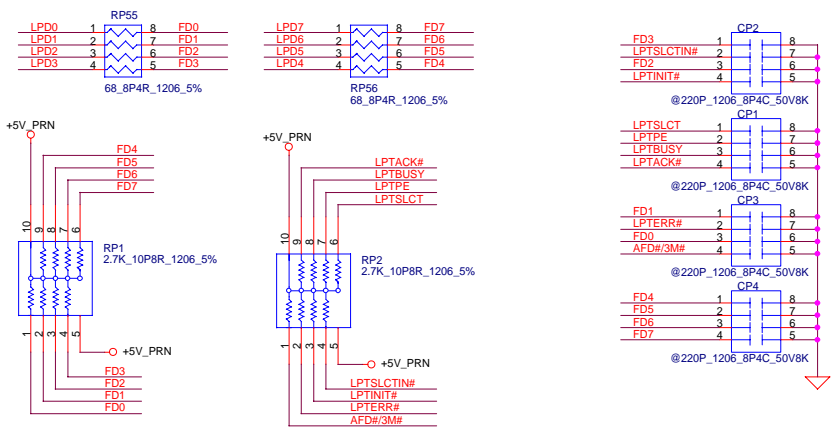
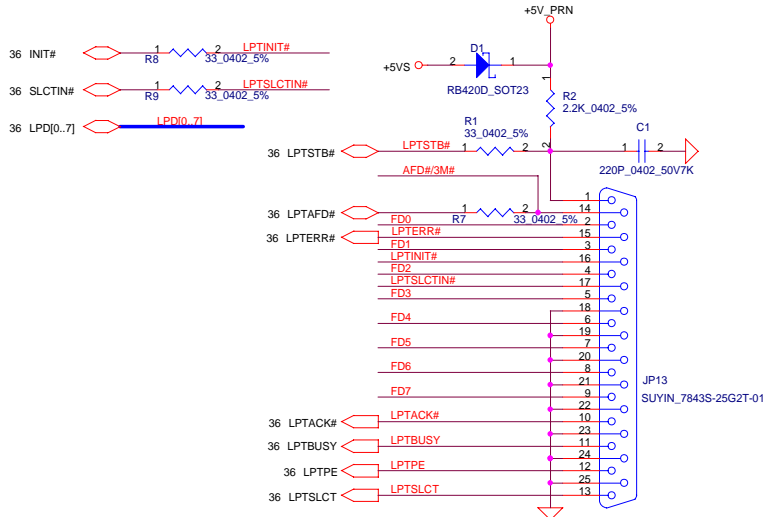
Compal Electronics, Inc.		
Title		
USB Conn.		
Size	Document Number	Rev
Custom	LA-2101	0.1
Date:	Saturday, November 22, 2003	Sheet 37 of 52

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MDC CONN.

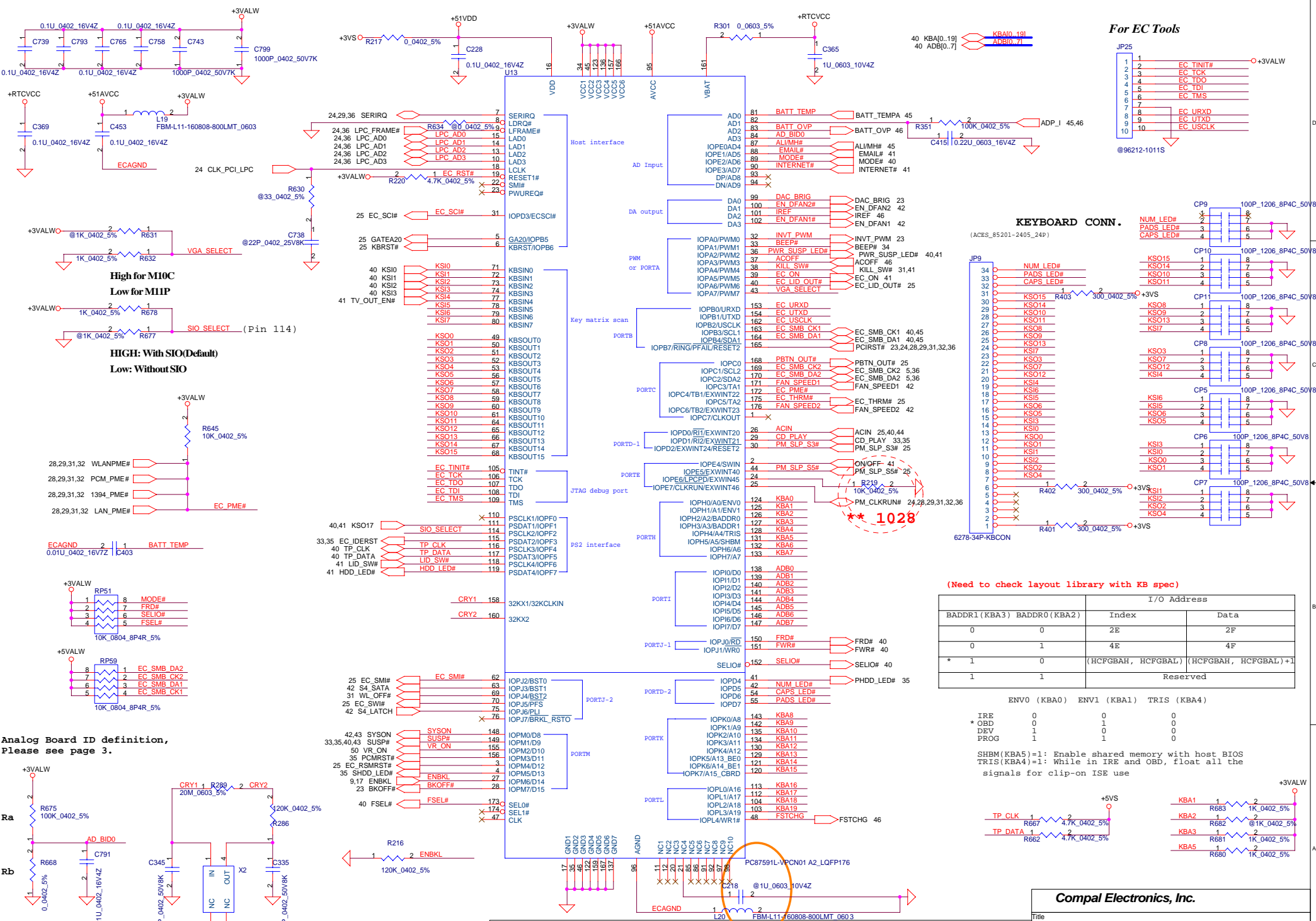


PARALLEL PORT

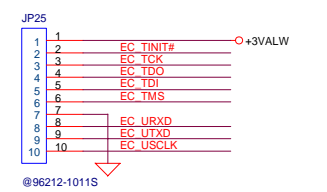


Compal Electronics, Inc.		
Title		
PARALLEL/MDC PORT		
Size	Document Number	Rev
	LA-2101	0.1
Date:	Saturday, November 22, 2003	Sheet 38 of 52

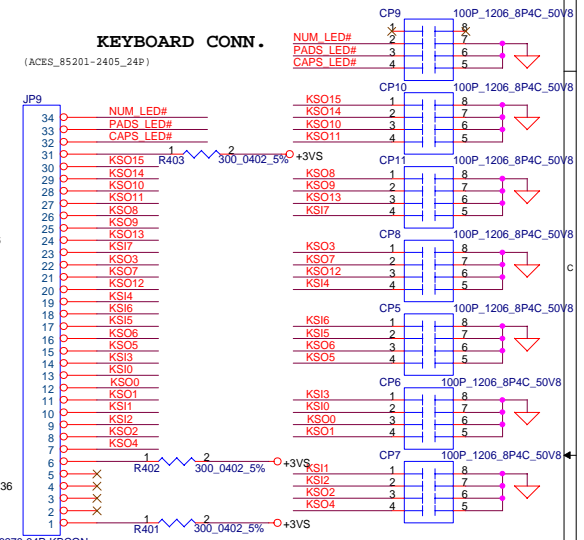
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For EC Tools



KEYBOARD CONN.

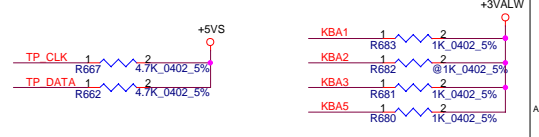


(Need to check layout library with KB spec)

I/O Address			
BADDR1 (KBA3)	BADDR0 (KBA2)	Index	Data
0	0	2E	2F
0	1	4E	4F
* 1	0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1	1	Reserved	

ENVO (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE	0	0
* OBD	1	0
DEV	1	0
PROG	1	0

SHBM(KBA5)=1: Enable shared memory with host BIOS
 TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use



Compal Electronics, Inc.

Title: **EC PC87591**

Size: Document Number

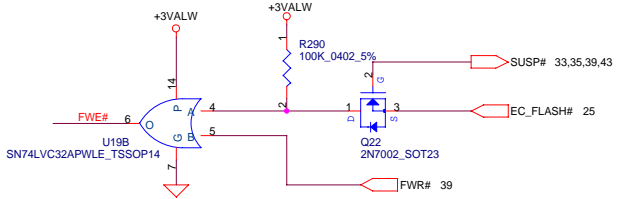
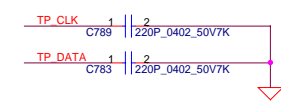
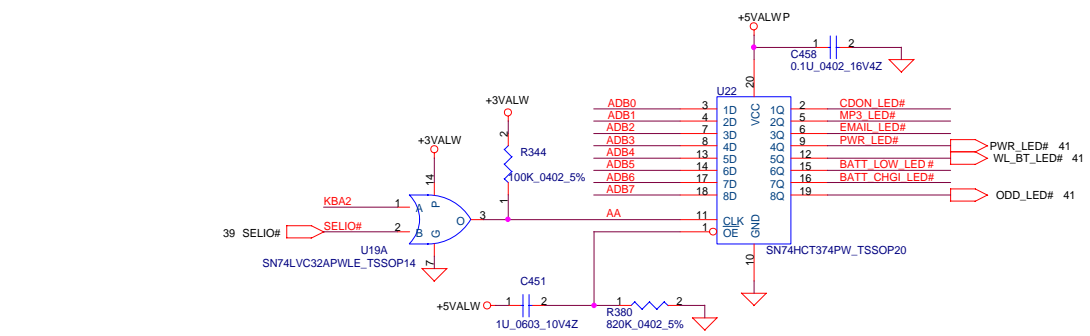
Custom: **LA-2101**

Date: Saturday, November 22, 2003

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Rev: 0.1

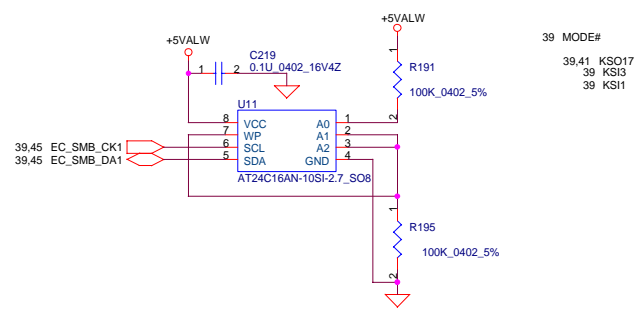
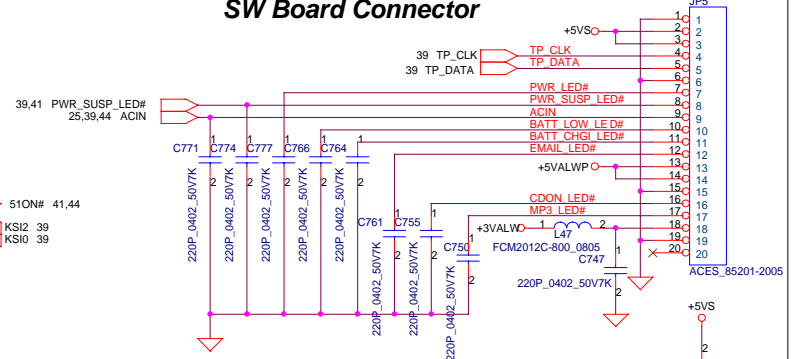
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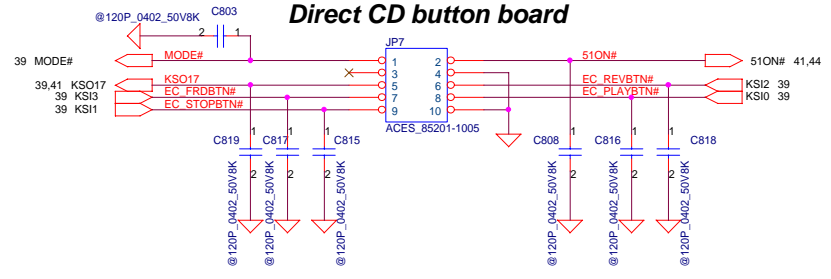
SW/B and TP/B FFC Connector
Pin 1 Definition Same As SW/B and TP/B

VR/B FFC Connector
Pin 1 Definition Swap with VR/B

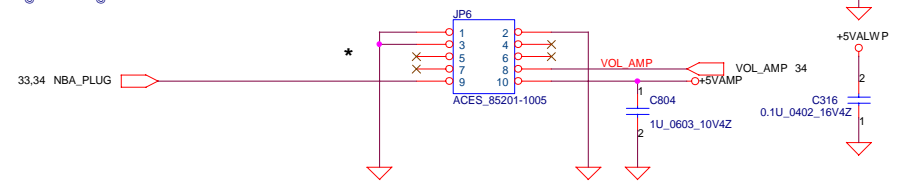
SW Board Connector



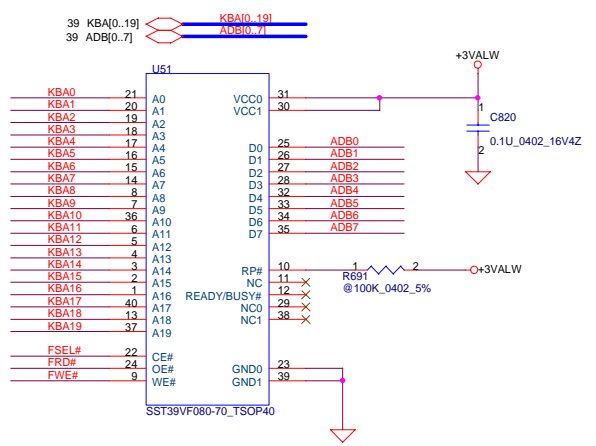
Direct CD button board



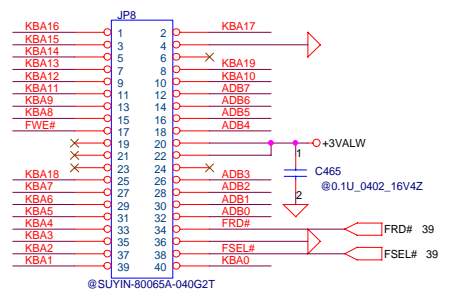
VR/CIR Board Connector



1MB Flash ROM



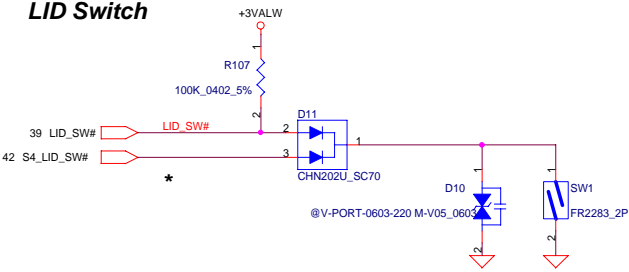
1MB BIOS Connector



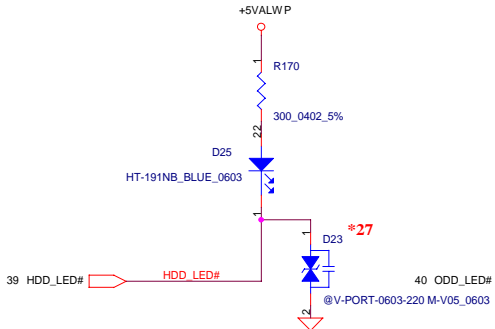
Compal Electronics, Inc.		
Title		
BIOS & EXT. I/O PORT		
Size	Document Number	Rev
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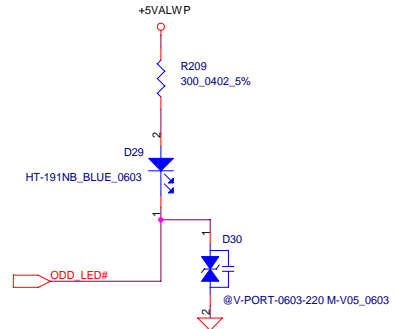
LID Switch



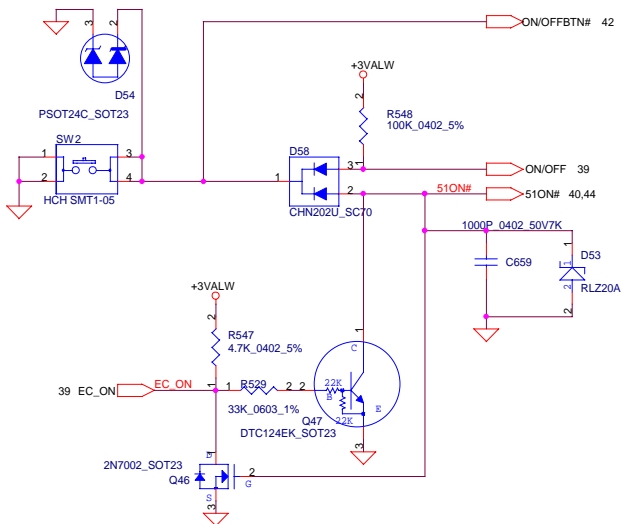
HDD LED



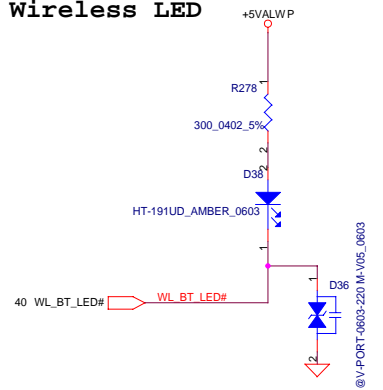
ODD LED



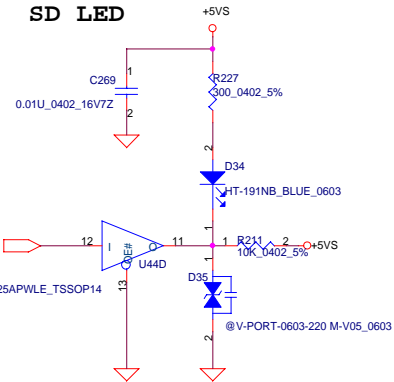
Power Button



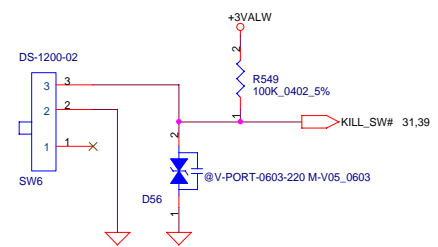
Wireless LED



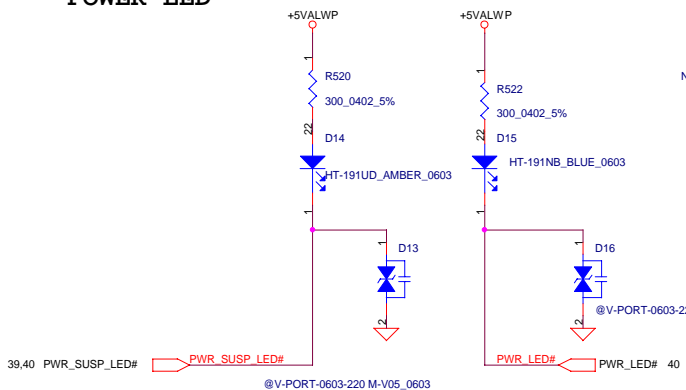
SD LED



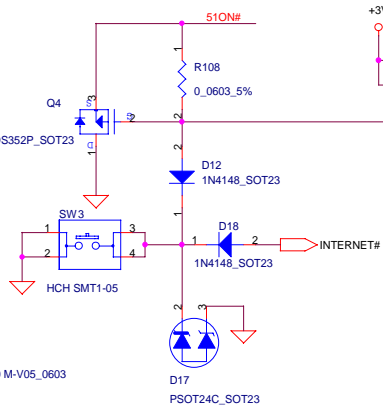
Kill Switch



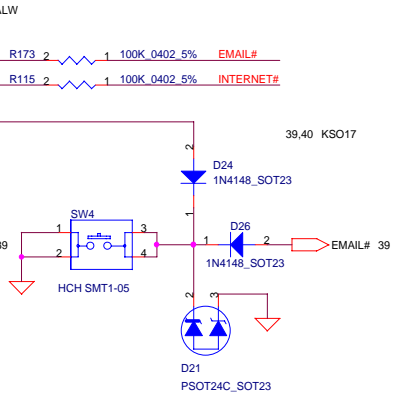
POWER LED



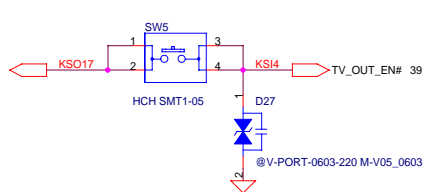
Internet Button



Console/E-MAIL Button



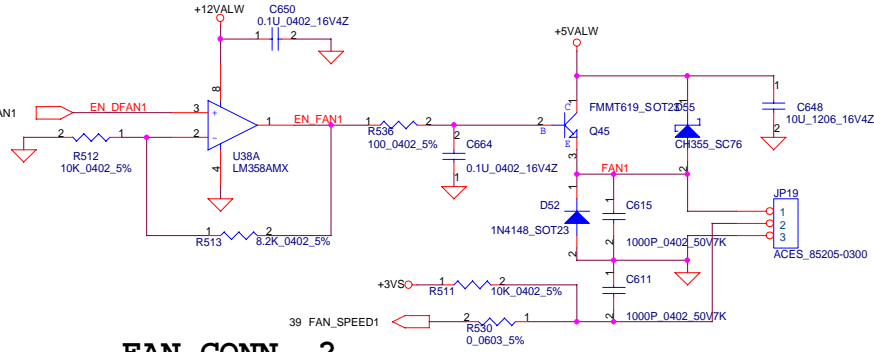
TV OUT Button



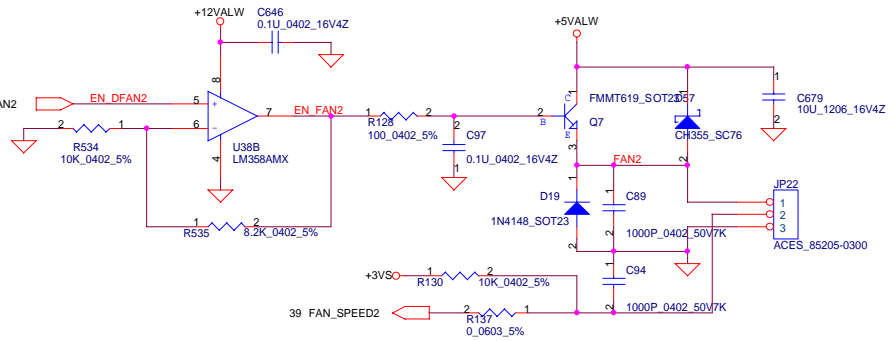
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Compal Electronics, Inc.		
Title		
Switches & Connectors		
Size	Document Number	Rev
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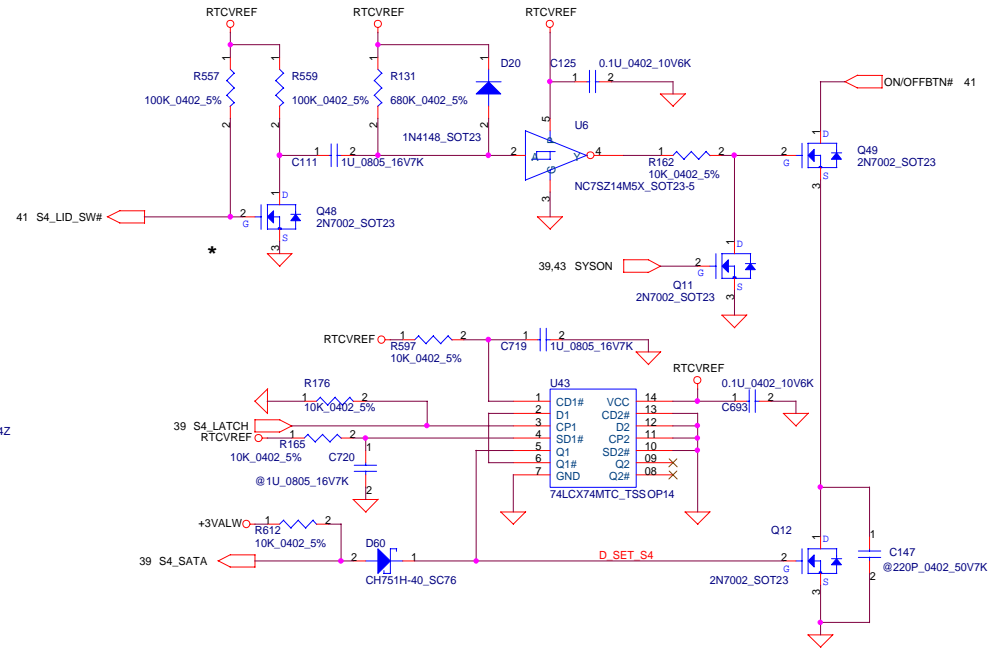
FAN CONN. 1



FAN CONN. 2

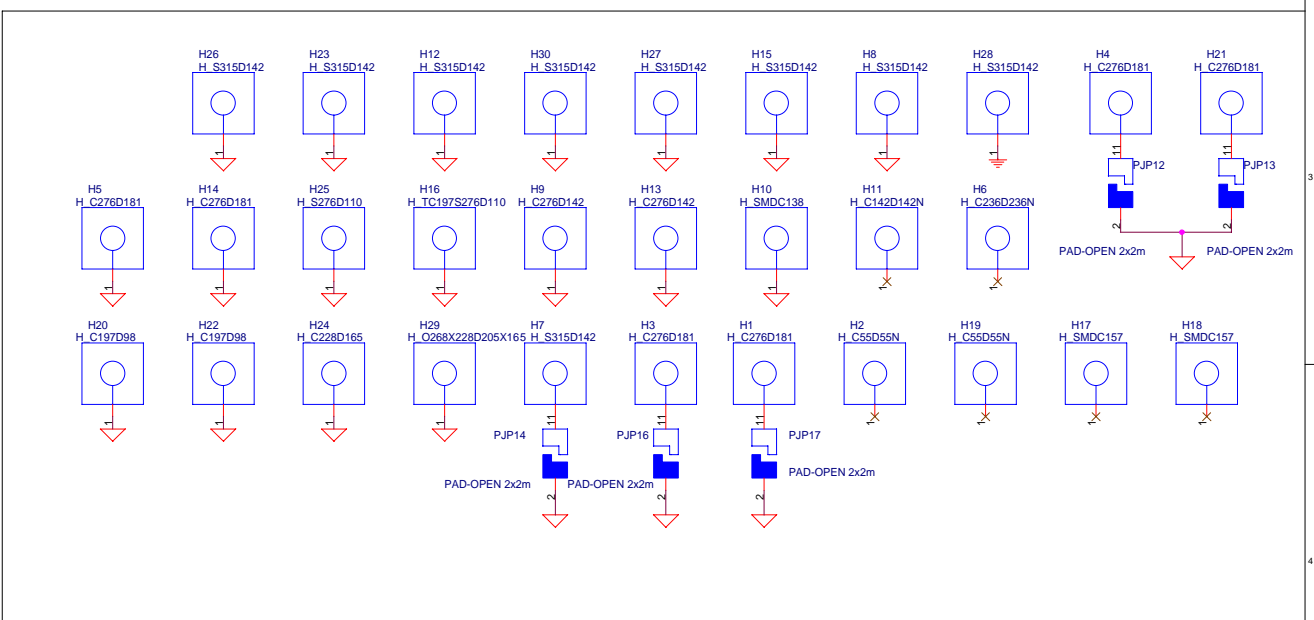
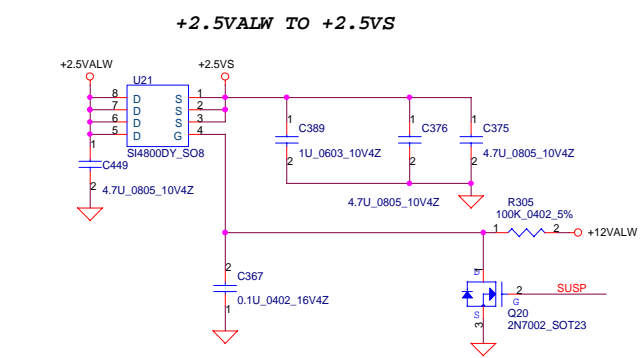
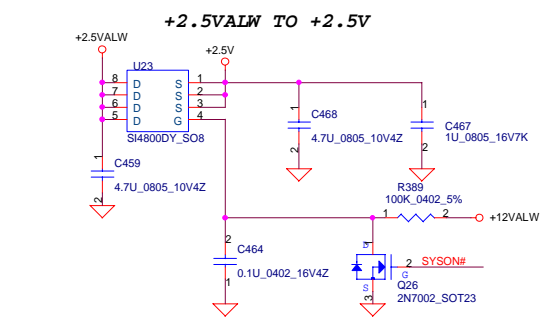
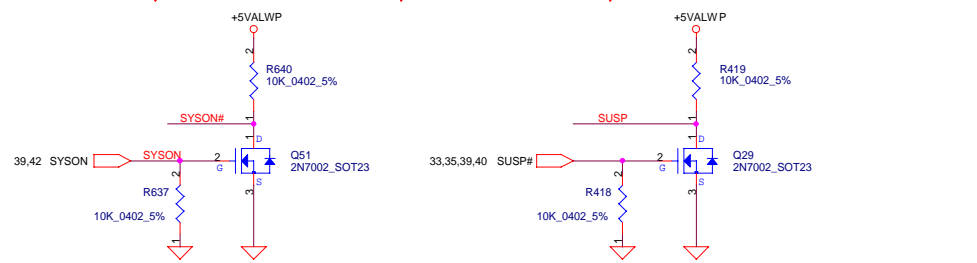
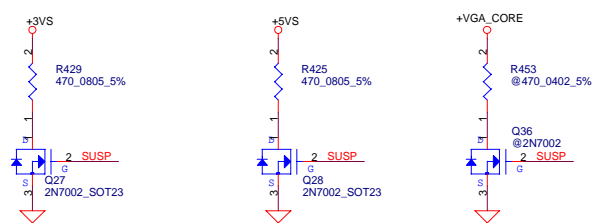
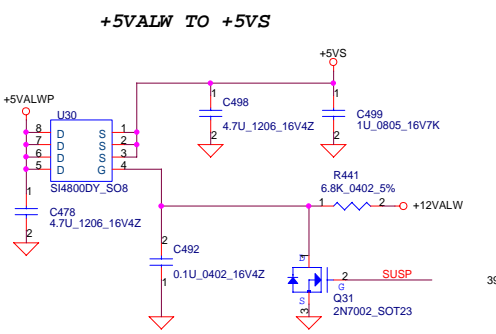
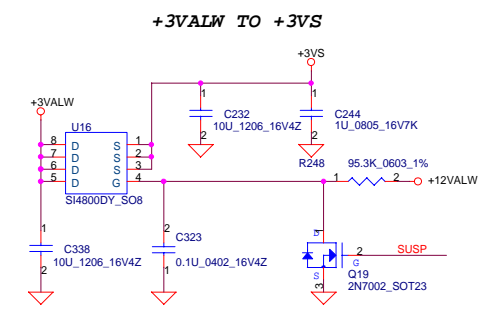
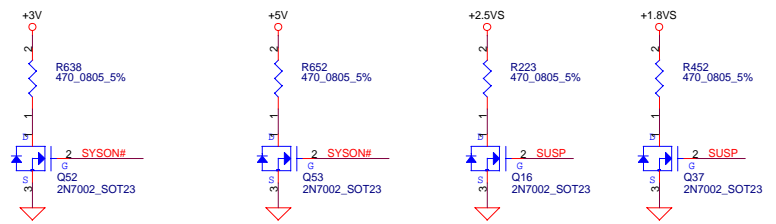
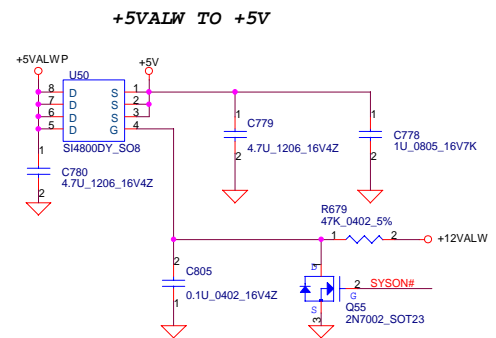
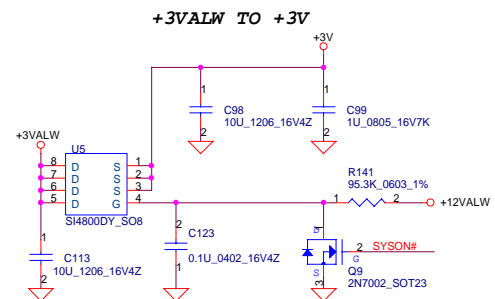


Battery mode Hibernation



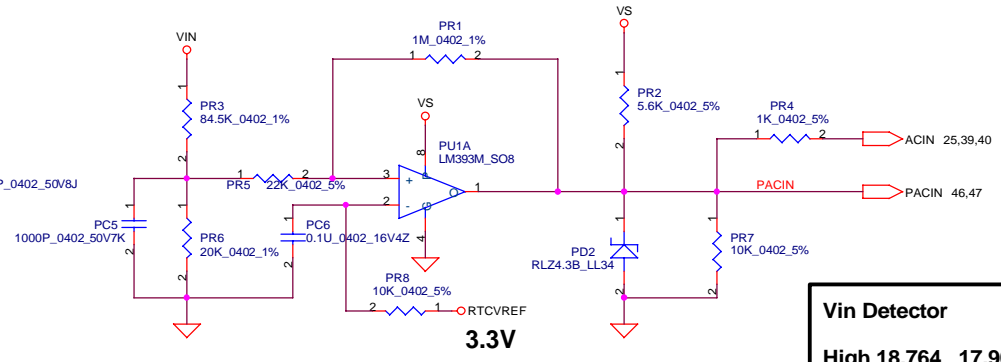
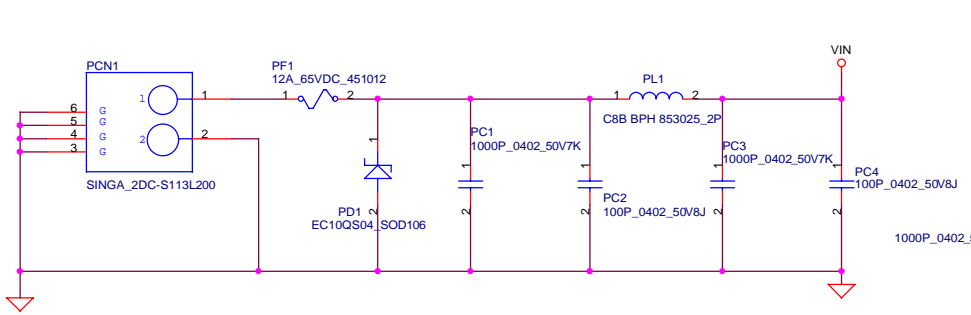
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Compal Electronics, Inc.		
Title Power OK/Reset/RTC battery/Lid Switch/Int. KB		
Size	Document Number LA-2101	Rev 0.1
Date	Saturday, November 22, 2003	Sheet 42 of 52

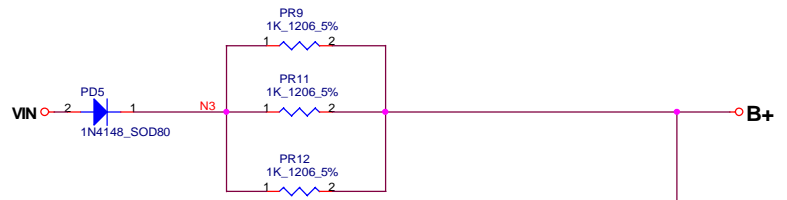
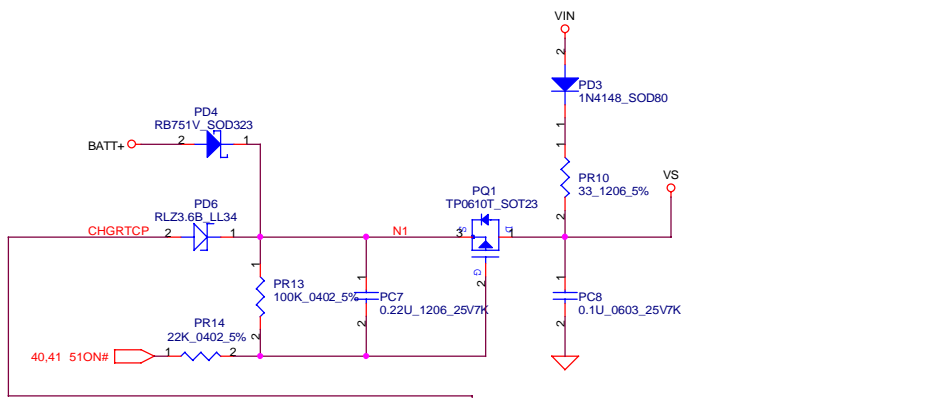


Compal Electronics, Inc.		
Title POWER CONTROL CKT		
Size	Document Number	Rev
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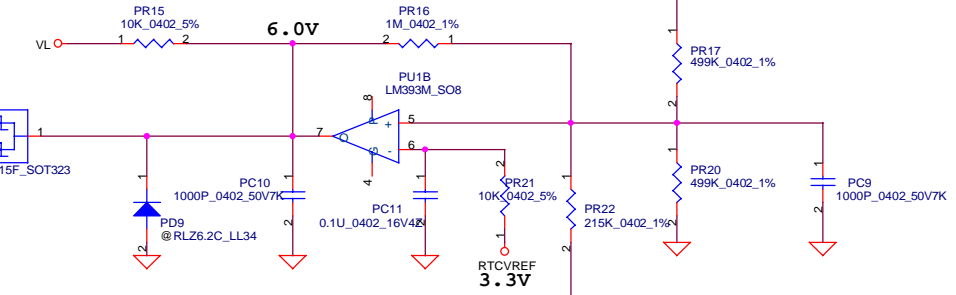
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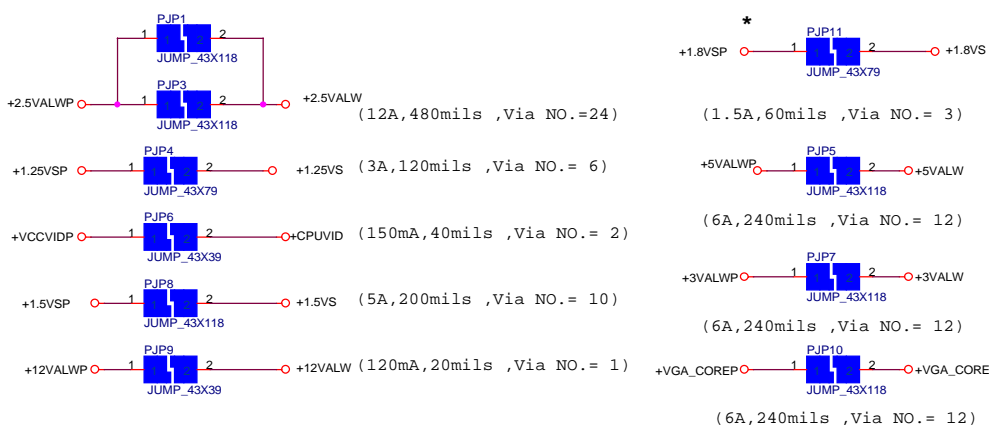
Vin Detector		
High	18.764	17.901 17.063
Low	17.745	16.903 16.038



6,45,47 MAINPWON
46 ACON

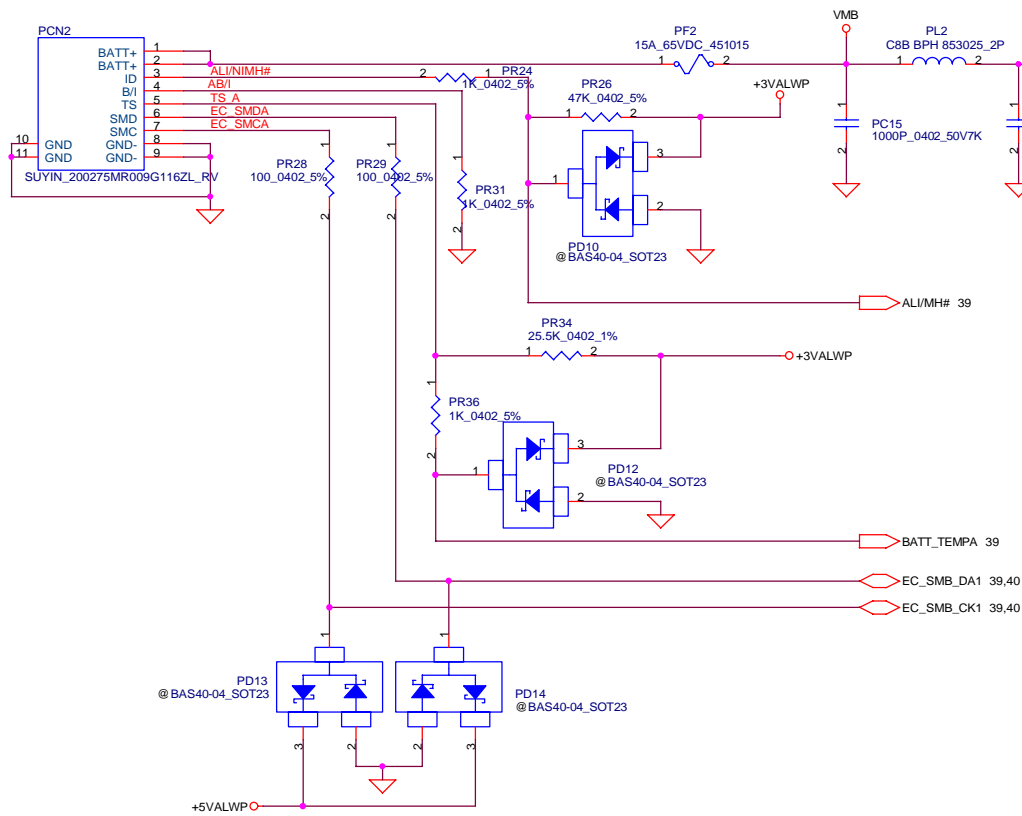


Precharge detector		
15.34	15.90	16.48
13.13	13.71	14.20

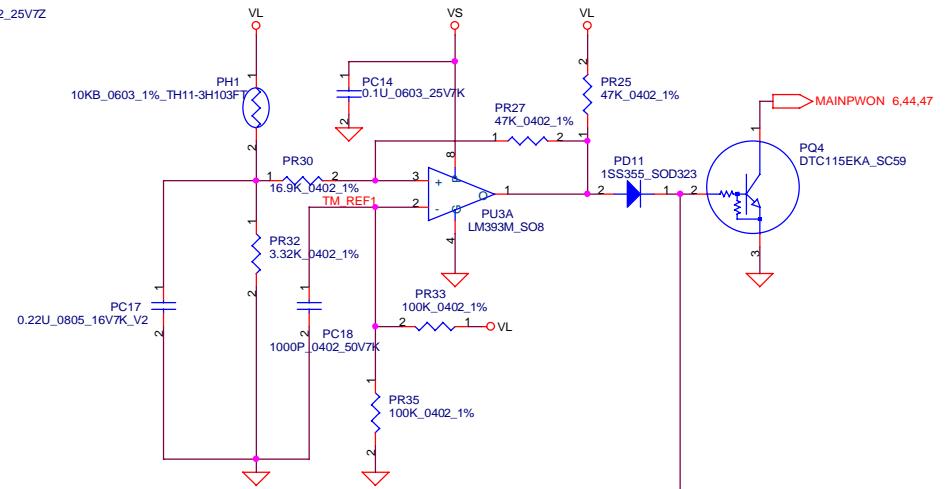


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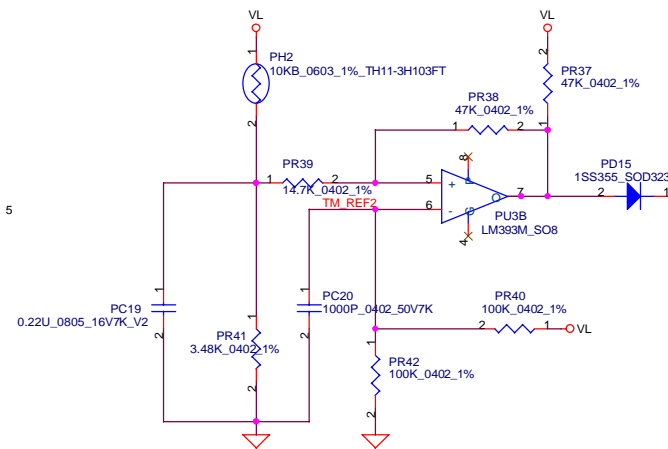
Compal Electronics, Inc.		
DCIN / DETECTOR		
Title	Document Number	Rev
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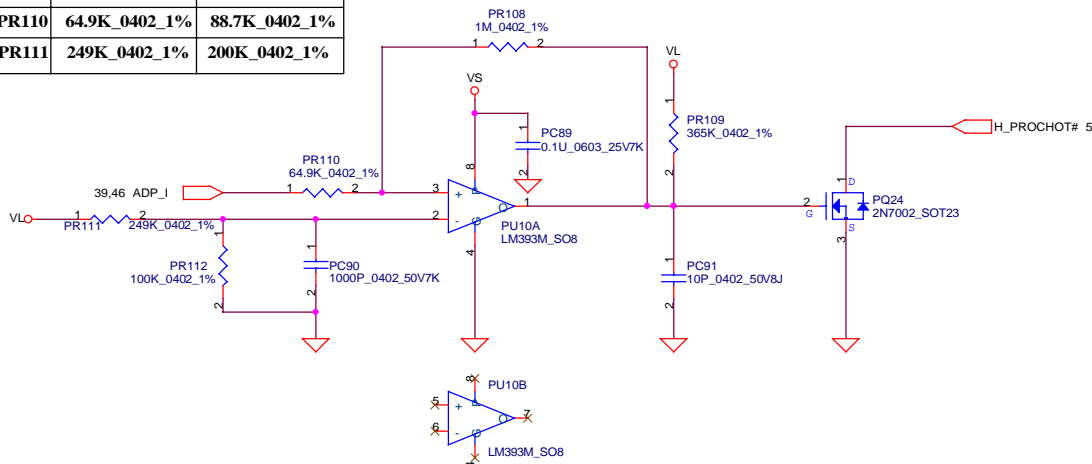
PH1 under CPU botten side :
 CPU thermal protection at 84 degree C
 Recovery at 44 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 78 degree C
 Recovery at 44 degree C



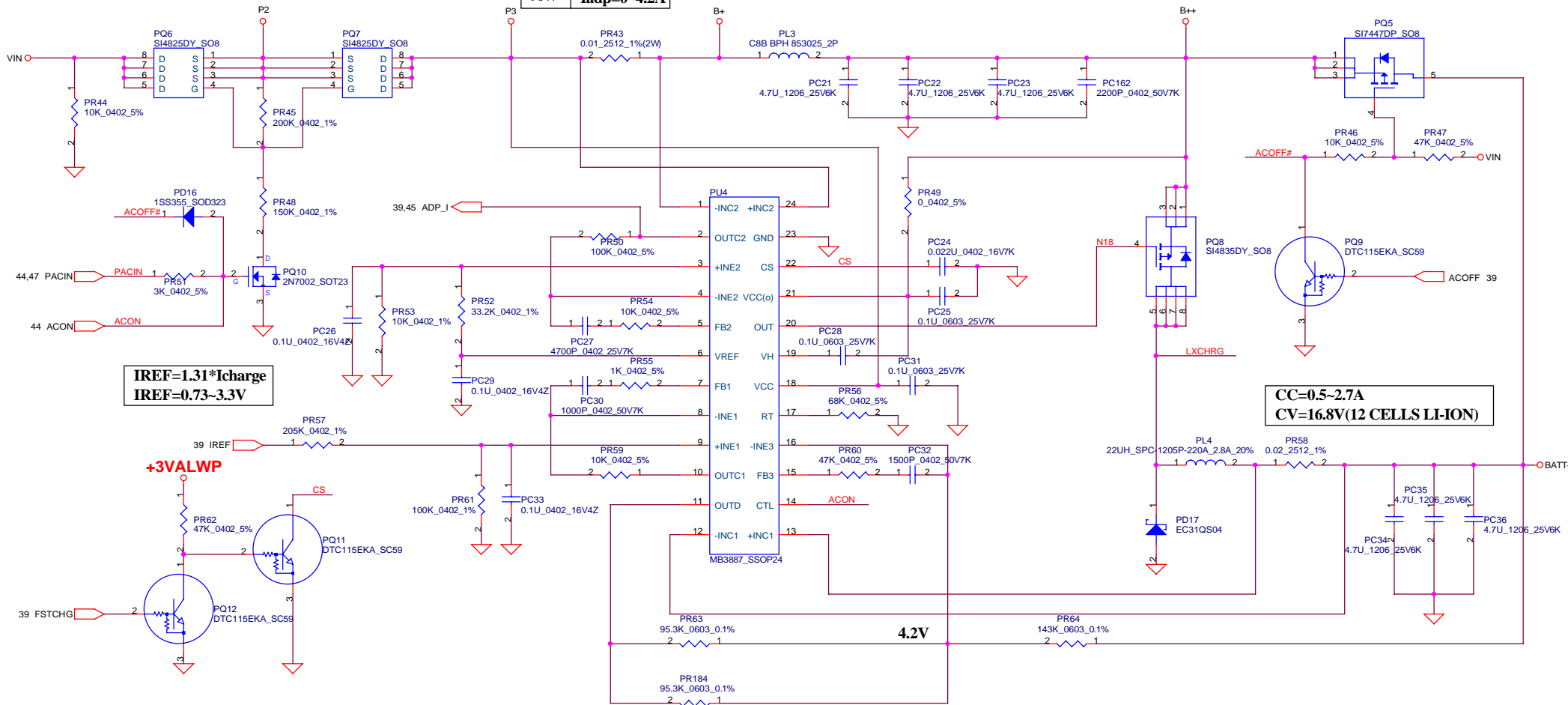
	120W	90W
PR109	365K_0402_1%	205K_0402_1%
PR110	64.9K_0402_1%	88.7K_0402_1%
PR111	249K_0402_1%	200K_0402_1%



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Compal Electronics, Inc.			
Title BATTERY CONN/OTP/Throttling			
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	LA-2101	0.1	
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120W	Iadp=0-5.8A
90W	Iadp=0-4.2A

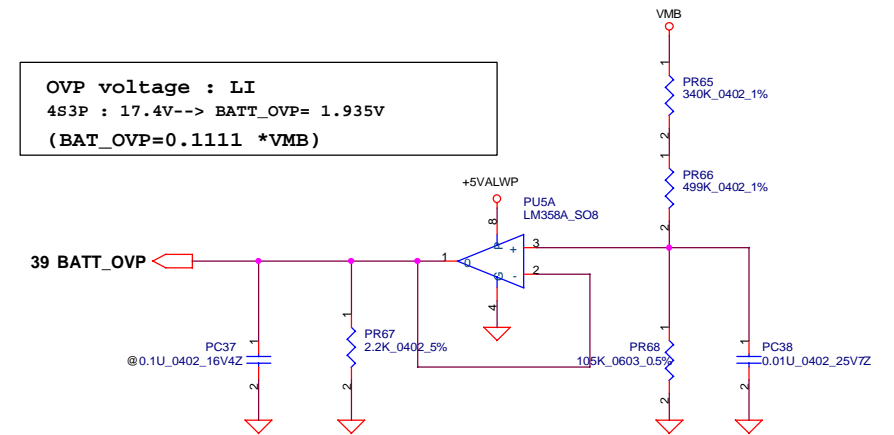


IREF=1.31*Icharge
IREF=0.73-3.3V

CC=0.5-2.7A
CV=16.8V (12 CELLS LI-ION)

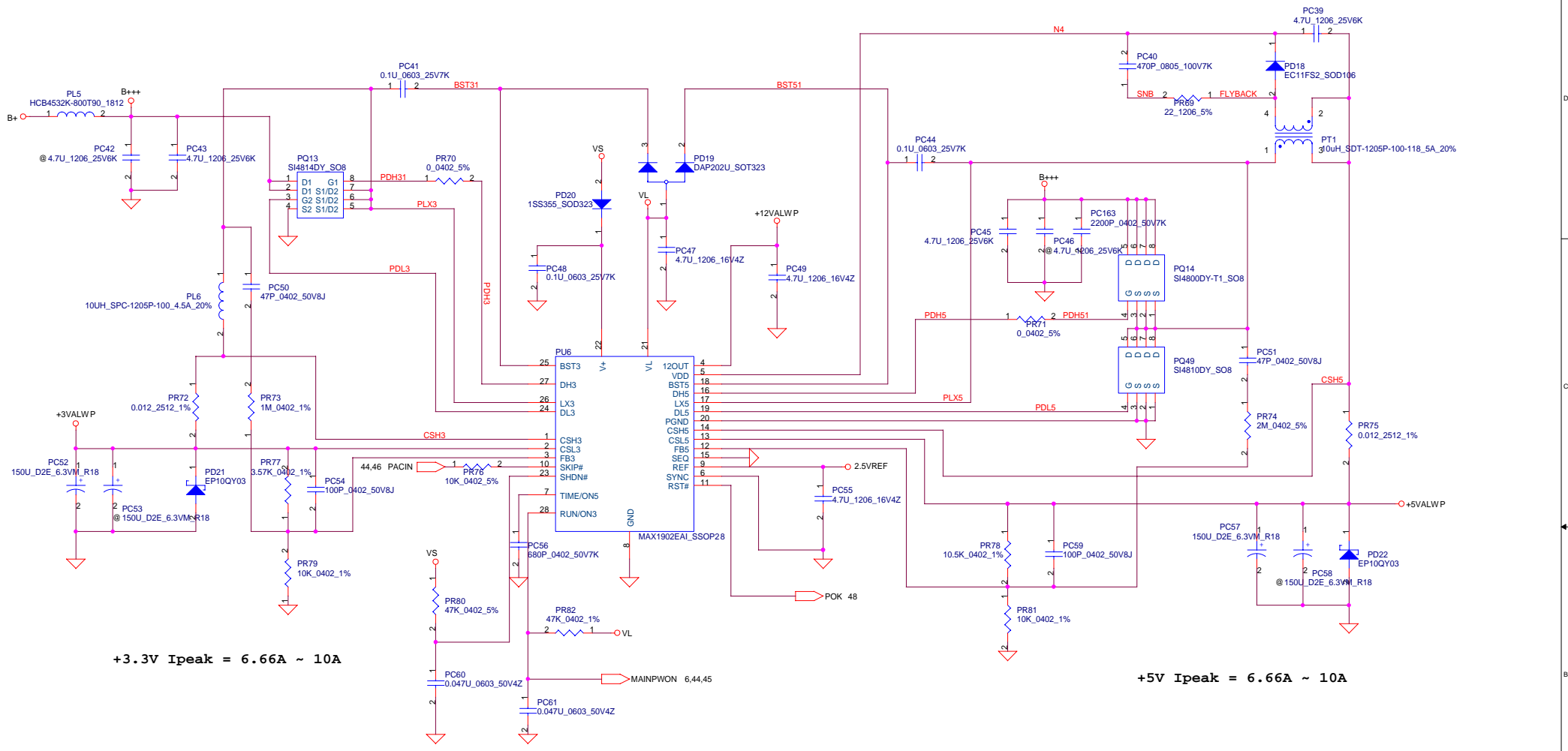
OVP voltage : LI
4S3P : 17.4V--> BATT_OVP = 1.935V
(BAT_OVP=0.1111 *VMB)

	PR43	PR52	PQ5
120W	0.01_2512_1%	33.2K_0402_1%	SI7447DP_SO8
90W	0.015_2512_1%	29.4K_0402_1%	SI4825DY_SO8



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Compal Electronics, Inc.		
CHARGER		
Size	Document Number	Rev
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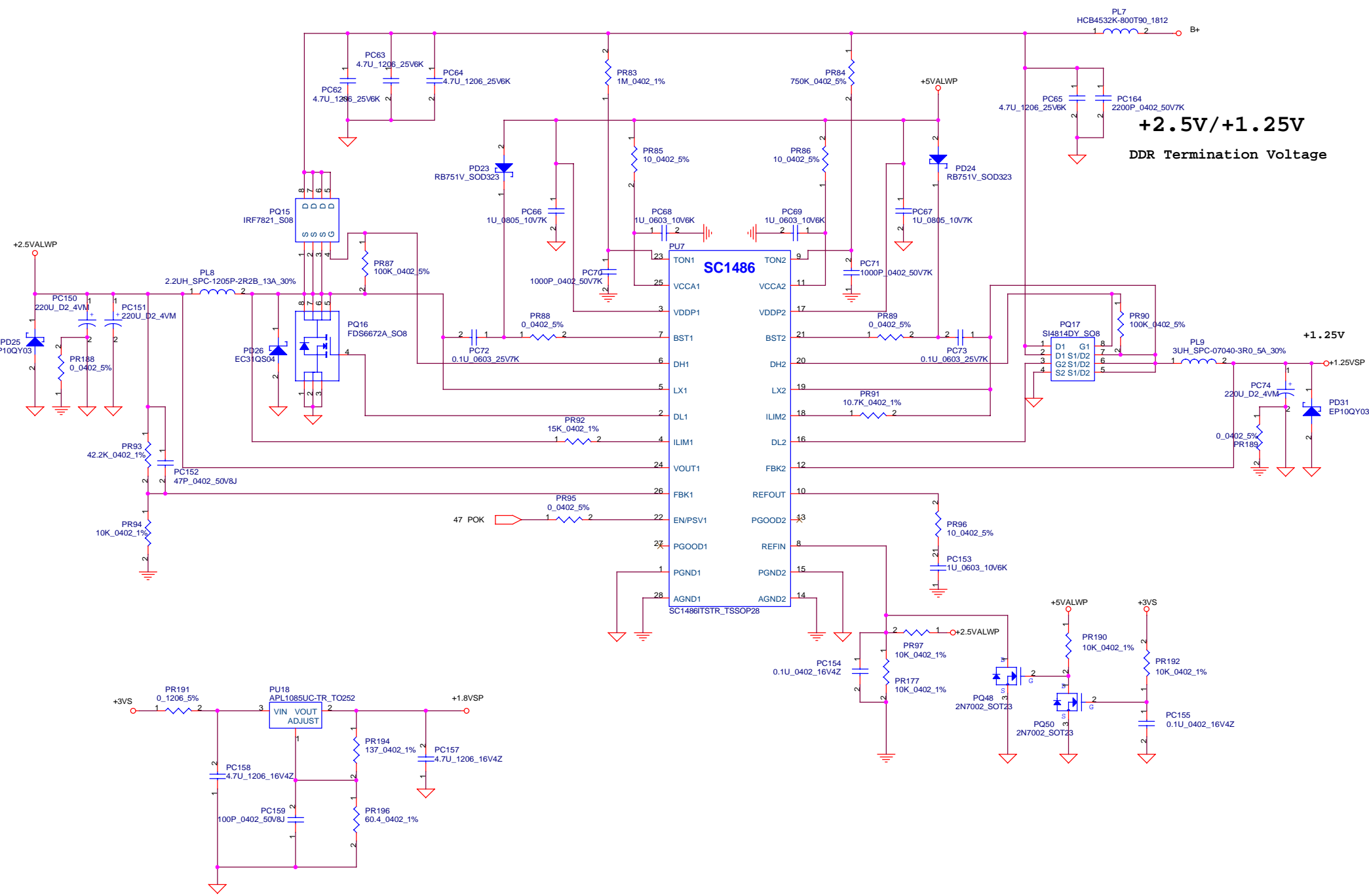


+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

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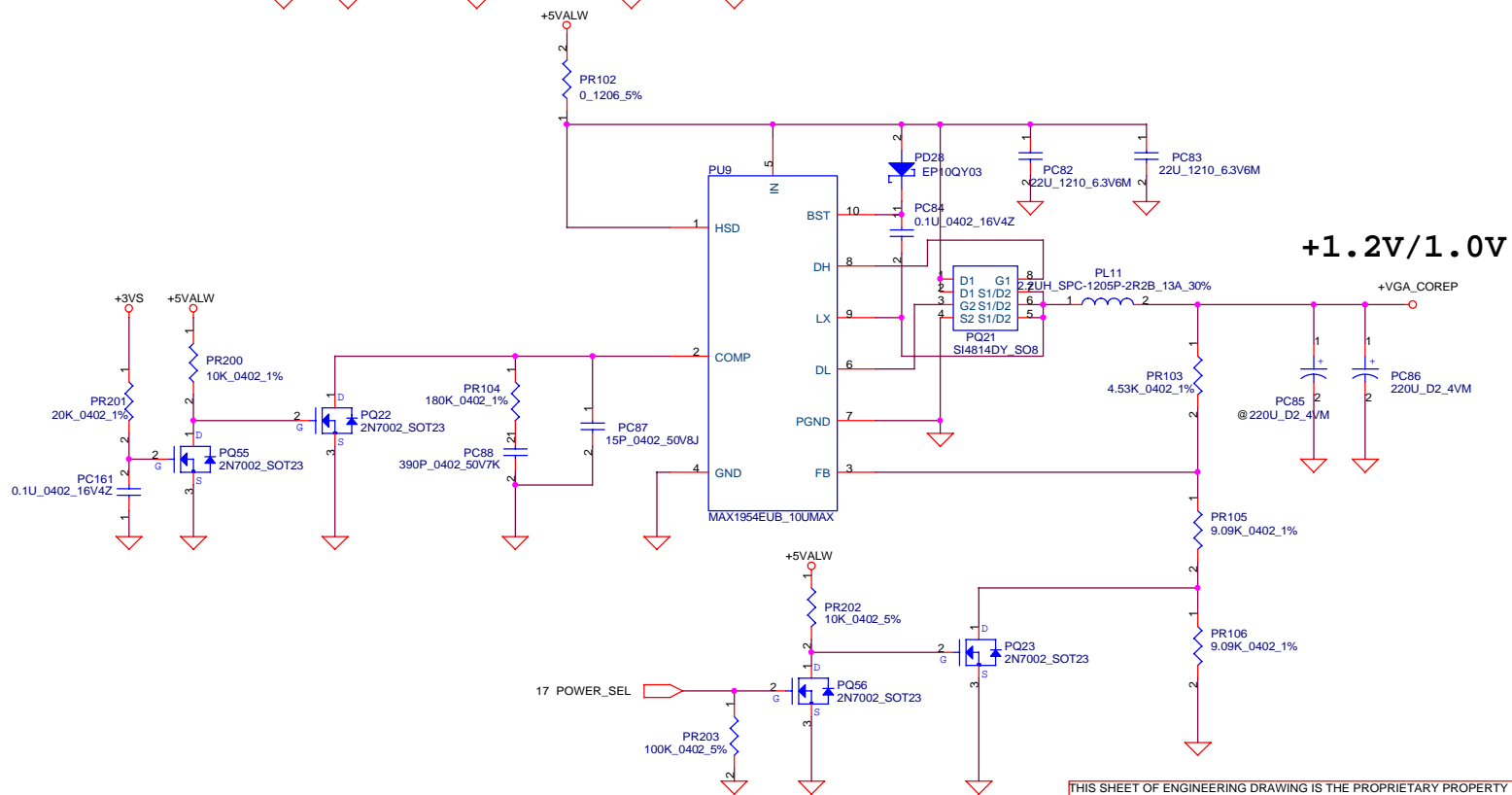
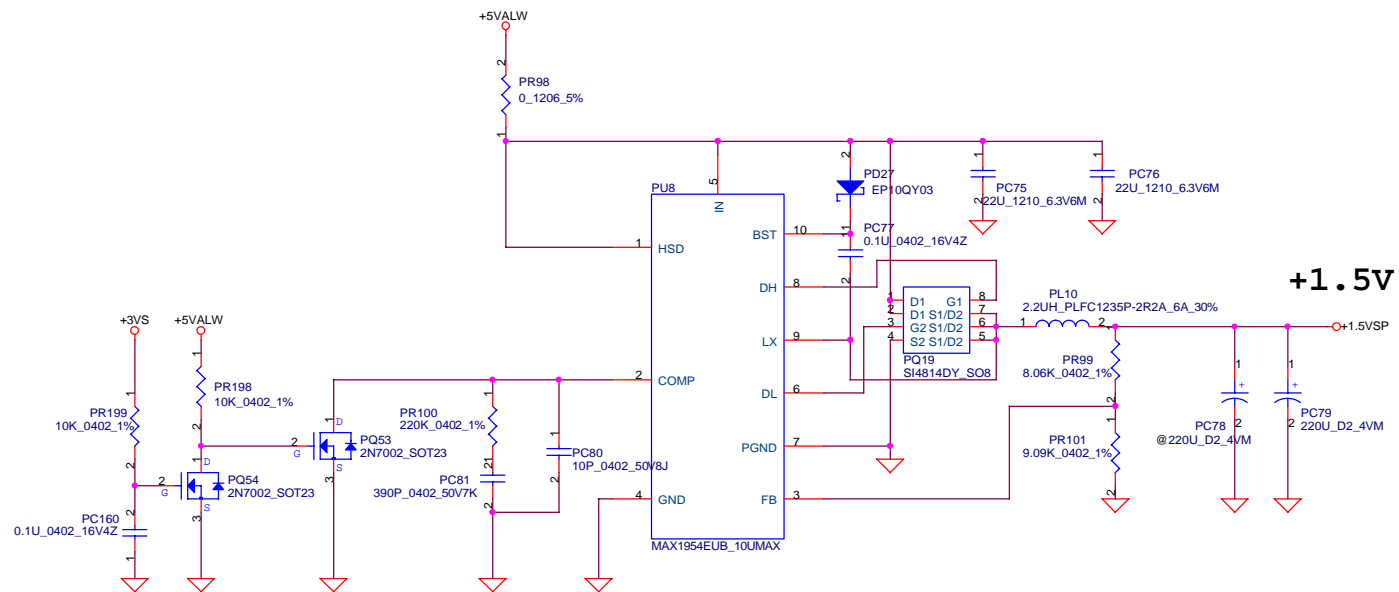
Compal Electronics, Inc.		
Title 5V/3.3V/12V		
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+2.5V/+1.25V
DDR Termination Voltage

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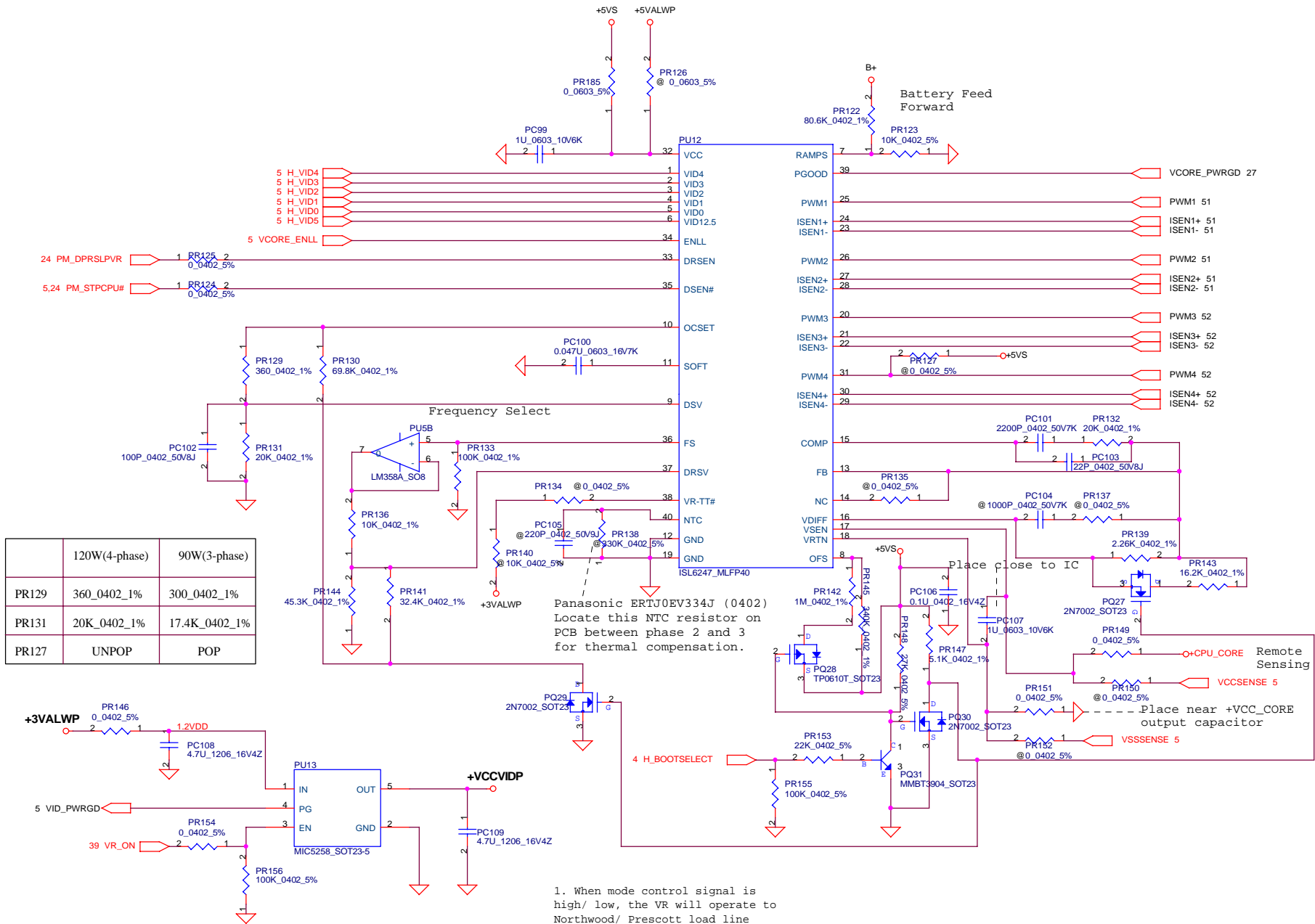
Compal Electronics, Inc.			
Title DDR_2.5V/1.25V/1.8V			
Size	Document Number	Rev	
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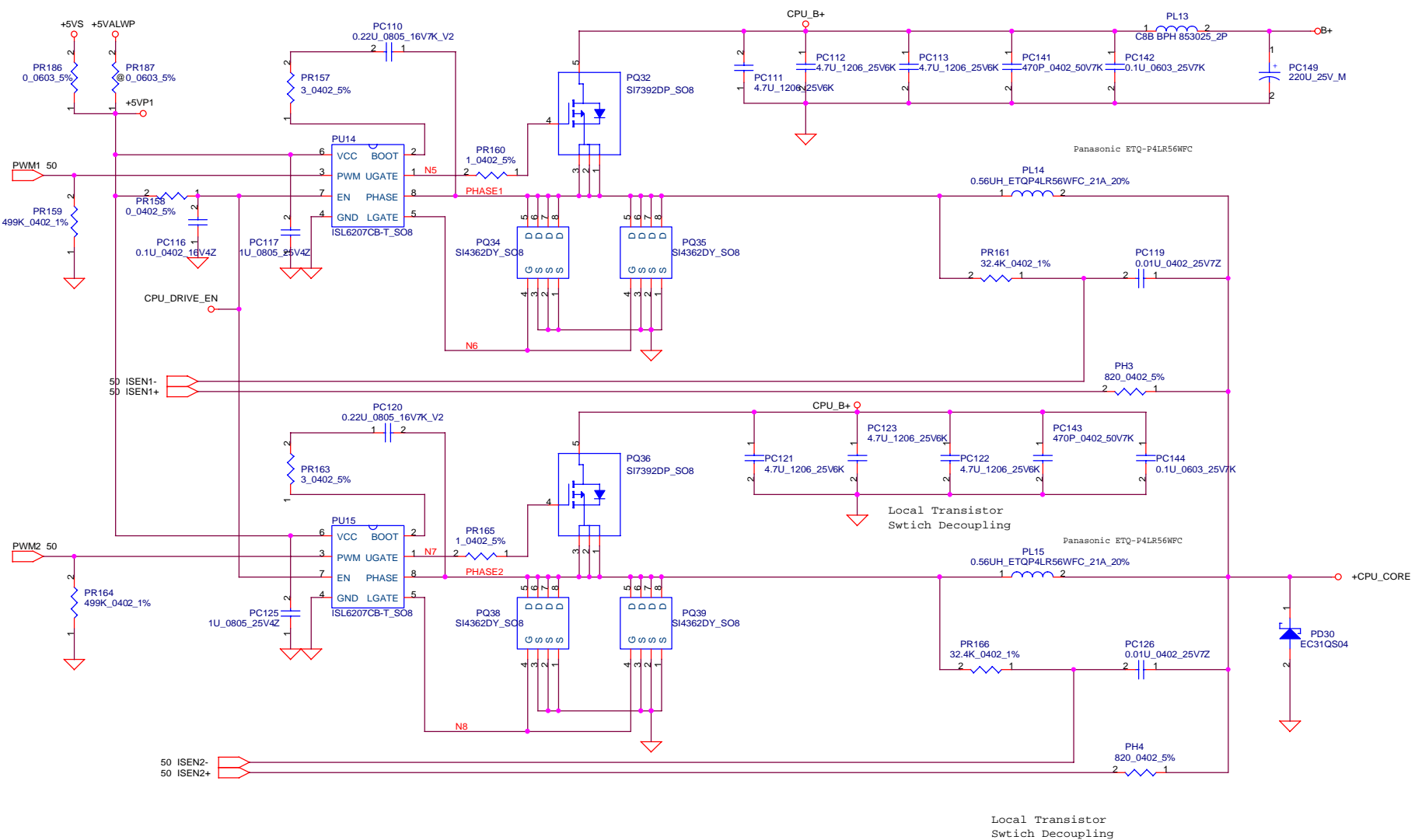
Compal Electronics, Inc.		
15V/VGA_CORE		
Size	Document Number	Rev
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	120W(4-phase)	90W(3-phase)
PR129	360_0402_1%	300_0402_1%
PR131	20K_0402_1%	17.4K_0402_1%
PR127	UNPOP	POP



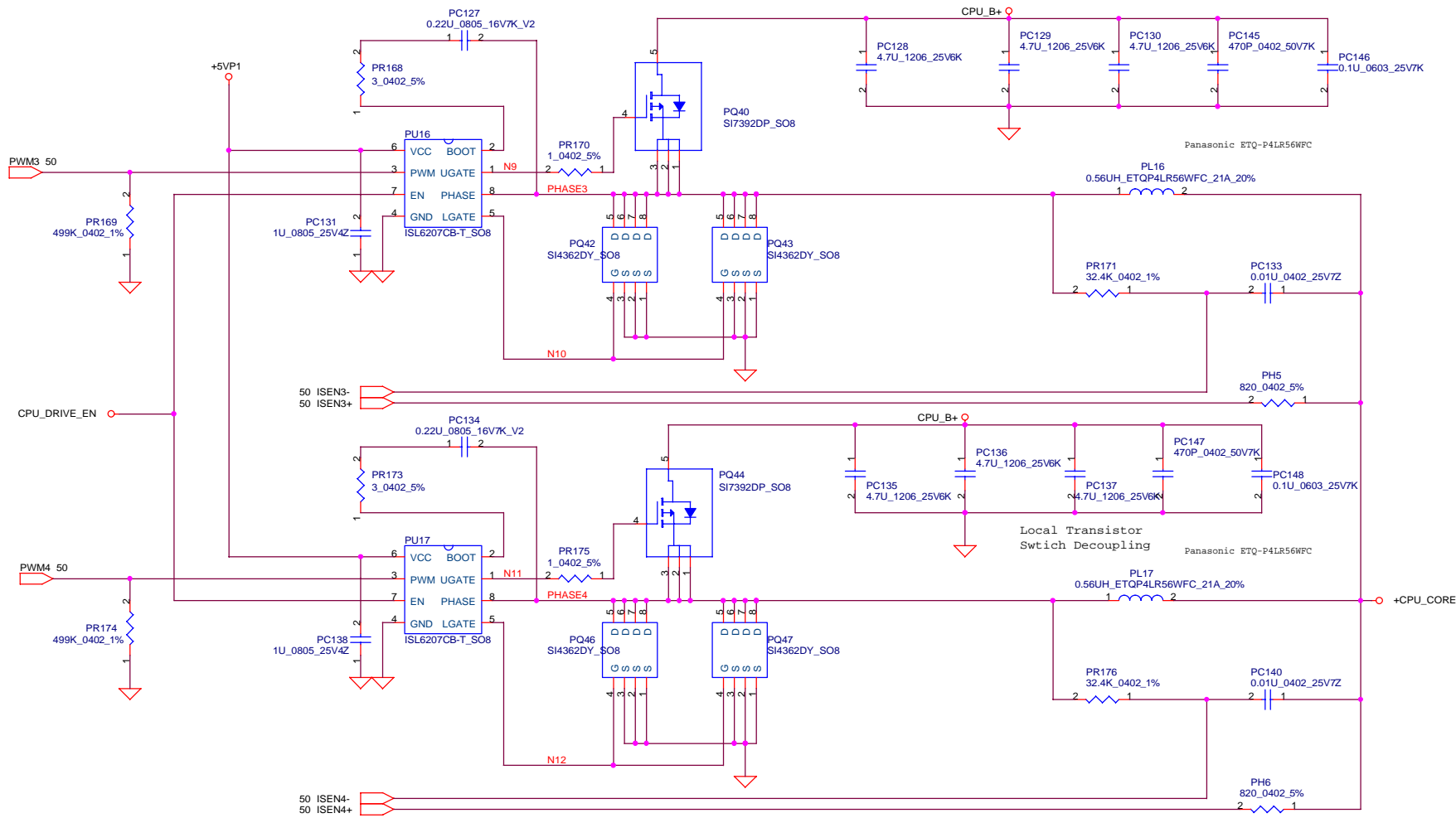
1. When mode control signal is high/ low, the VR will operate to Northwood/ Prescott load line (Northwood="0", Prescott="1")
2. VID5(12.5) should be pulled high, when the VR operates to Nothwood load line.

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Compal Electronics, Inc.			
CPU_CORE Power stage 1			
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	PC134,PC135,PC136,PC137,PC138,PC140, PC147,PC148,PR173,PR174,PR175,PR176, PQ44,PQ46,PQ47,PU17,PL17,PH6
120W(4-phase)	POP
90W(3-phase)	UNPOP

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